Reconfiguration of Wireless Sensor Node In Fpga

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Abstract
Sensor networks are usually deployed in dynamic environments where each node must adapt itself to changes.
The objective of this paper is to design reconfigurable wireless sensor node in FPGA. The idea behind node reconfigurability is that the network can adapt its functionality to the current situation, in order to lessen the use of the scarce energy and memory resources, while maintaining the integrity of its operation. The reconfiguration has been done using Mobiroute protocol and data is transferred between two nodes using OFDM transceiver. The node has been tested using Xilinx ISE Design tools. The modules of Mobiroute protocol and OFDM transceiver have been done in VHDL

Keywords—Mobiroute protocol, Node reconfiguration, OFDM transceiver, WSN

1. INTRODUCTION

A WIRELESS sensor network (WSN) is a network of small sensor nodes, characterized by features like easy to deploy, harmless, multiple use, and economical. The WSN is being used in many applications today, e.g., habitat monitoring, disaster management, inventory management, medical diagnosis, structural monitoring, and agriculture. In most of the applications, sensor nodes are battery driven, and the energy consumption of the sensor node determines the battery life. A good compromise between hardware inflexibility and software inefficiency can be found in low-power programmable logic. Reprogrammable logic can be utilized to find efficient paths by detecting link failure and detect loss of packets in the receiver side. Reconfigurable sensor platforms offer flexibility and cost-effective customization before deployment and provide for the possibility of run-time reconfiguration.

ASICs are specifically designed for a target application, and even though they can provide the best performance, but due to the lack of flexibility to accommodate design changes and long design-to-fabrication cycles they cannot be used in a sensor node. Another option is a general-purpose processor. This type of processor provides the flexibility that the ASIC cannot offer, but at the price of reduced processing speed and power efficiency. FPGA can be reconfigured and reprogrammed according to the requirements.

Digital Signal Processors may be chosen for broadband wireless communication applications, but in Wireless Sensor Networks the wireless communication is often modest: i.e., simpler, easier to process modulation and the signal processing tasks of actual sensing of data is less complicated. Therefore the advantages of DSPs are not usually of much importance to wireless sensor nodes. FPGAs can be reprogrammed and reconfigured according to requirements.

II. RECONFIGURATION USING MOBIROUTE PROTOCOL

According to the definition of discrete mobility pattern , the sink changes its location from time to time. A routing protocol that transfers data towards such a sink should perform the following operations :

1) Notify a node when its link with the sink gets broken due to mobility.
2) Inform the whole network of the topological changes incurred by mobility.
3) Minimize the packet loss during the sink moving period.

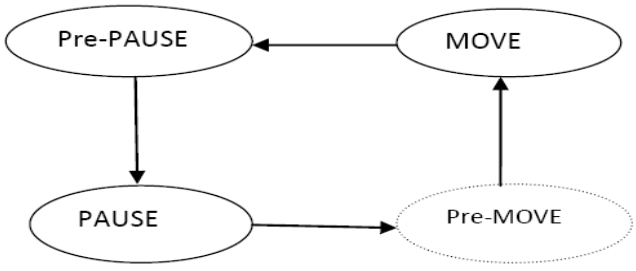

Fig.1. States and transitions involved in MobiRoute

The state diagram shown in Fig.1.is used when we present MobiRoute.The mobile sink can simply be a laptop (moved occasionally by a human), rather than a sophisticate robot as used. The flow diagram for Mobiroute protocol has been shown in Fig.3.

A. Detecting Link Breakage

In order to inform the nodes located close to the sink trace about the state of their links with the sink, MobiRoute applies a bit stream mechanism. The source periodically broadcasts a bit stream. A sink node, upon receiving a bit stream sets (or resets) its detecting timer. If the timer times out before receiving the next bit stream, the failure detector at this node indicates a link breakage and a new sink node is chosen.

It is required that the sink to transit from the pause state to the pre-move state before physically beginning to move. The sink begins to broadcast bit stream under the pre-move state and evolves to the move state after a while. The sink moves while broadcasting bit stream- under the move state. A node, after receiving the first bit stream under its current pause state, transits to the move state directly. Nevertheless, the pre-move state (of the sink) is necessary: it guarantees the reception of bit stream at the nodes' side before
the link quality changes due to the sink mobility.

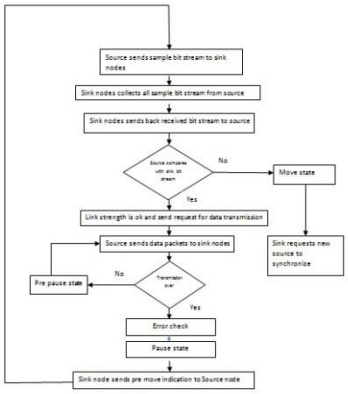

Fig.2. Flow diagram of Mobiroute Protocol

B. Conveying Topological Changes

Propagating information throughout a network is a costly procedure, it cannot be performed frequently. So MobiRoute only performs propagation upon the sink reaching an anchor, and it tolerates a limited number of sub-optimal routing during the moving period. The sink enters the pre-pause state when it stops moving; it then sends route messages with a speed-up rate, which causes their receivers to enter the same state. Nodes that receive messages directly from the sink should synchronize with other sink; they re-evaluate the quality of their links with the sink using these synchronization. A node upon synchronization indirectly also enters the pre-pause state; it forwards the message only if its distance towards the sink changes significantly

C. Detecting Packet Losses

Cyclic prefix is a module, which is used to concatenate partial end of information bit and put at the beginning of the information frame. A cyclic prefix is an important feature of OFDM and is used to combat ISI and ICI effects introduced by the multi-path channel through which the signal is propagated. This results in a continuous, cyclically-extended signal at the seam of two serialized OFDM symbols,
as illustrated in Fig.3., thanks to the periodic nature of the FFT. The duration of the guard period, TG , (corresponding to NGI samples) should be longer than the worst-case delay spread of the multi-path channel in question. At the receiver, the demodulator will effectively 'see' an incoming OFDM symbol with an integral number of cycles within the FFT window, thanks to the cyclic prefix. Therefore, orthogonality will be preserved and ICI should not occur.

A guard interval reduces data throughput as a percentage of the total received time-domain OFDM signal is not used for data transmission. The sampling instant, TX , is chosen such that τ max < TX < TG , where τ max is the maximum delay spread of the channel. Provided this condition is satisfied, there will be no ISI as the effects of the previously transmitted symbol will only be present on the channel for received signal samples within the range [0,τ].max .

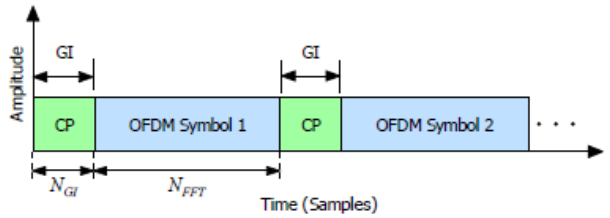

Fig. 3. Time domain representation of a sequence of OFDM symbols with cyclic prefix (CP) guard intervals.

III.OFDM TRANSCEIVER

Orthogonal Frequency Division Multiplexing (OFDM) is a multi-carrier transmission technique, which divides the available spectrum into many carriers, each one being modulated by a low rate data stream.

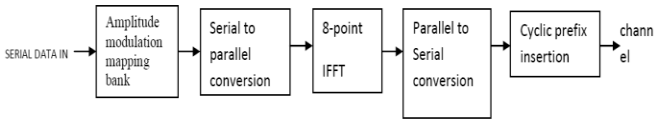

Fig. 4. Simplified transmitter block diagram

Fig.4. above show the simplified block diagram of OFDM transmitter. It can be seen that the block is divided into several parts with each block function differently and this is to ensure that the system works effectively. Since the main component is processing block, so, the work is started from this part. All block set function is implemented in the FPGA development board.

The generation of OFDM signal started from amplitude modulation mapping bank. The serial input data is mapped to appropriate symbol to represent the data bits. These symbols are in serial and need to convert into parallel format since IFFT module requires parallel input to process data. The serial to parallel module does the conversion. These parallel symbols are transformed from frequency domain into time domain using IFFT module. These signals are converted into serial format and add a cyclic prefix to data frame before being transmitted. The receiving process will be the reverse process of the transmission process as shown in Fig. 5.

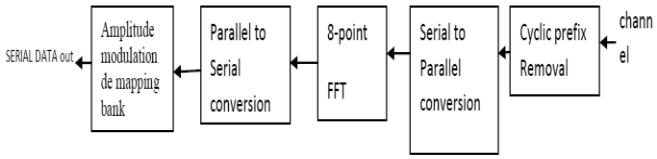

Fig. 5. Simplified Receiver block diagram

A. FFT and IFFT Algorithms

The discrete Fourier transform (DFT) X_k of an N-point discrete-time signal x_n is defined by:

$$X_k = \sum_{n=0}^{N-1} x_n W_N^{nk}, \qquad 0 \le k \le N-1 \tag{1}$$

In equation (1) $W_N = e^{-j\pi 2/N}$ which is commonly referred to as the twiddle or phase factor.

For instance, an input signal multiplied by W^2_{16} in Fig. 6 can be expressed as:

$$(a + jb)W_{16}^2 = \sqrt{2}[(a+b) + j(b-a)]/2, \tag{2}$$

where $(a + jb)$ denotes a discrete-time signal in complex form.

Similarly, the complex multiplication of W^6_{16} is given by:

$$(a + jb)W_{16}^6 = \sqrt{2}[(b-a) - j(a+b)]/2. \tag{3}$$

Both these above equations will ease hardware implementation in the future, because they only need to calculate the multiplication by √2 / 2 and two real additions, respectively. Especially, the multiplication by √2 / 2 can be obtained easily, which circuit design will be introduced in the latter section.
The inverse discrete Fourier transform (IDFT) of length *N* is given by:

$$x_n = \frac{1}{N}\sum_{k=0}^{N-1} X_k W_N^{-nk}, \qquad 0 \le n \le N-1 \tag{4}$$

To reuse the same hardware core for reducing the chip area (4) can be rewrite as:

$$x_n = \frac{1}{N}\left(\sum_{k=0}^{N-1} X_k^* W_N^{nk}\right)^*, \qquad 0 \le n \le N-1 \tag{5}$$

Where the star symbol * denotes a conjugate.

Since $W_N^{3N/8} = W_N^{N/8}$, it can be given by either the multiplication by $W_N^{N/8}$ first and then the multiplication by $-j$ or the reverse of the previous calculation.

The designed hardware utilizes this kind of cascaded calculation and multiplexers to realize all the necessary calculations of the PE1 stage. This saves a bit-parallel multiplier in PE1 stage for computing $W_N^{3N/8}$, which further forms a low-cost hardware.

IV. SIMULATION IN XILINX ISE SUITE

After designing the wireless sensor node , the design has been simulated using Xilinx ISE tool

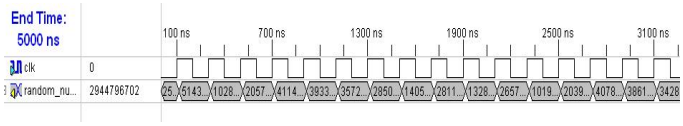

Fig.6. Random Generator Output

Fig.6. shows the randomly generated data, which will be the input data for the wireless sensor node. The random generator automatically generates 32 bit random values

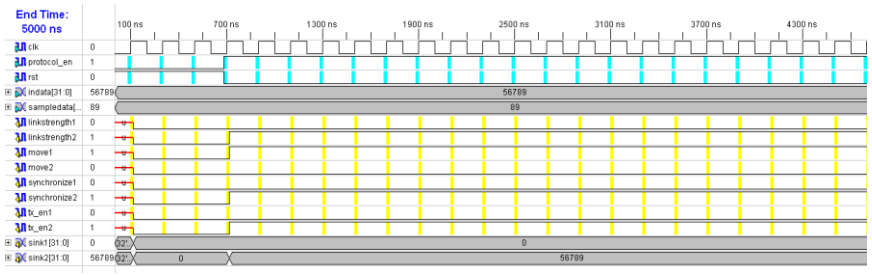

Fig.7. Detection of link breakage

In Fig.7 the link breakage from source to sink 1 is indicated by linkstrength 1, which is low. Due to this link failure source is finding another sink, here sink 2 which will be acting as an intermediate node for source and sink1. The presence of link between source and sink2 is indicated by linkstrength2, which is high. The sink node 2 is receiving the data which is same as that of the input data.

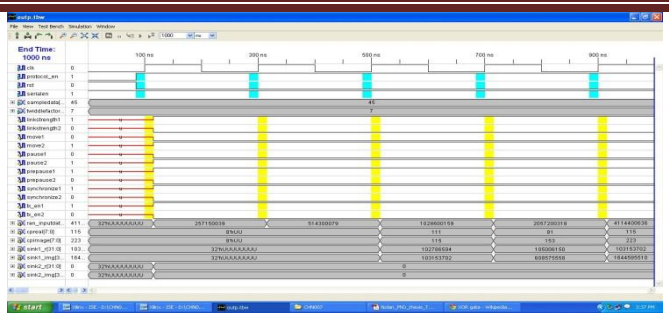

Fig.8. Transmitter output

In Fig.8, the sink 1 is ready to receive the data that is indicated by link strength1 , synchronize1 and tx_en1,which are high. The pause state and move state are indicated as low.Sink1 has received the data after adding cyclic prefix value. The random generator value is the data to be transmitted.

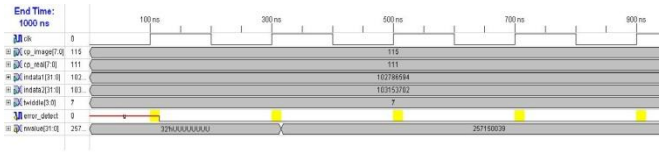

Fig.9. Receiver output

In Fig.9.the received output is same as that of the random generator value, in Fig.8. Since the received data and transmitted data are same the error_detect is indicated as low
If both of the values are not same, the error_detect will be high.

V. Conclusion

The Wireless sensor node for reconfiguration has been designed and has been implemented in Spartan II . All the modules have been designed in VHDL and simulated using Xilinx ISE tool.

References

[1] JunLuo, Jacques Panchard, Michal Piorkowski, MatthaisGrossglauser, Jean- Pierre Hubaux, "MobiRoute : Routing towards a Mobile Sink for Improving Lifetime in Sensor Networks", 2006

[2] Stefan Dulman1, Tjerk Hofmeijer2, Paul Havinga, **"**Wireless sensor networks dynamic runtime configuration", 2004

[3] Joel L. Wilder, Vladimir Uzelac, Aleksandar, Milenkovic,and Emil Jovanov, **"**Runtime, Hardware Reconfiguration in Wireless Sensor , Networks",2007

[4] KoustubhKulkarni, SudipSanyal, "Dynamic. Reconfiguration of Wireless Sensor Networks"'2009

[5] Gowrishankar.S., T.G.Basavaraju, SubirKumar Sarkar, **"**Simulation Based Analysis of Mobile Sink Speed in Wireless Sensor Networks",2010.

[6] Xin Yu Niu, "Reconfiguring Distributed Applications in, FPGA Accelerated Cluster with Wireless, Networking",2010.

[7] GopinathBalakrishnan, Mei Yang, Yingtao Jiang and, Yoohwan Kim, "Performance Analysis of Error Control Codes for wireless Sensor Networks"2007.

[8] H.L. Groginsky and G.A. Works, "A pipeline fast, Fourier transform,"IEEE Transactions on, Computers, vol. C- 19, no. 11, pp. 1015-1019, Nov. 1970.

[9] KoushikMaharatna, Eckhard Grass, and Ulrich, Jagdhold, "A 64-Point fourier transform chip for high- speed wireless LAN application using OFDM," IEEE Journal of Solid-State Circuits, vol. 39, no. 3, pp. 484- 493, Mar. 2004.