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Floating Gate MOSFET Based Current Differencing Buffered Amplifier and Its Applications as Third-Order Filters

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ABSTRACT *: In this paper, a floating gate MOS (FGMOS) based current differencing buffer amplifier (CDBA) has been presented. The proposed CDBA operates at low supply voltage of ± 1.25 V and consumes minimum power of 2.78 mW. The maximum linear range for the current differencing unit is approximately – 700 µA to + 700 µA and for the voltage buffer unit it is − 1.2 V to + 1 V. Additionally, a third-order low pass (LP) and band pass (BP) filter are reported as applications of this suggested CDBA block. The proposed filter circuits use single CDBA, three capacitors, four/three resistors for LP/BP response. All the circuits are simulated using PSPICE in TSMC 250 nm technology.*

KEYWORDS: *Current differencing buffered amplifier (CDBA), third-order filter, voltage mode, current mode, FGMOS.*

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I. INTRODUCTION

Increasing need of portable devices and technology scaling, low-voltage low-power techniques have been gaining a great deal of attention. A lower supply voltage reduces the power consumption which increases the reliability and battery lifetime of the portable device. The supply voltage and power dissipation can be lowered by reducing the threshold voltage [1-3]. Various low voltage techniques such as sub-threshold MOSFETs, bulk-driven MOSFETs, self-cascode MOSFETs, level shifters, floating-gate MOSFETs (FGMOS) are available to minimize supply voltages. Among them, FGMOS is the most efficient technique as threshold voltage can be removed or reduced by supplying voltage at one of its control gates [1]. Using FGMOS transistors several analog circuits have been reported [1-5].

Presently, the designing of current mode active block has become a major issue due to good linearity, higher bandwidth, wide dynamic range, good slew rate, low power consumption, simple circuit configuration over the voltage mode circuits [5-6]. Current differencing buffered amplifier (CDBA) is a versatile current mode active block reported by Acar and Ozoguz in 1999 [7]. It offers both the voltage mode and the current mode outputs [8-13]. Furthermore, it is free from multiple parasitic capacitances, thus suitable for high frequency operation. It has been used to implement various circuits such as multiplier [8], oscillator [9-10], filter [10-12], squaring and square-rooting circuits [13] etc. There are different ways to implement CDBA [7, 14-20]. One possible implementation is based on the use of current feedback amplifiers (CFAs) [7]. In this case the property of CDBA is dominated by the characteristic of the CFA. The CDBA reported in [14] is based on bipolar technology. Various CMOS implementation of CDBA are also available in literature [15-20]. But the voltage gain of CMOS based CDBA are much less than one. In addition, most of them use large number of transistors [15, 16] and operated at high supply voltages [15-17]. Furthermore, the input linear ranges for [18-20] are low. A detailed comparison of the proposed CDBA and previously reported works is given in Table 1.

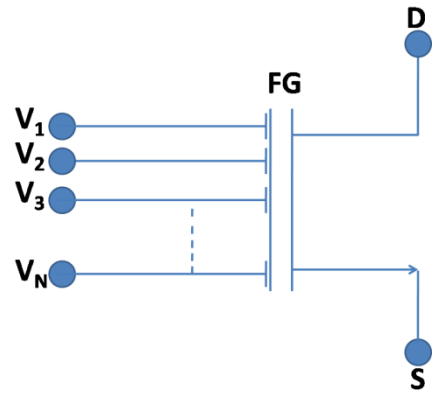
The main goal of this work is to design a high performance CDBA using FGMOSFETs. The design method is based on the modification of current differencing unit of [21] and a voltage buffer circuit of [2, 3]. Furthermore, using this proposed CDBA as an active element, a voltage mode third-order low pass and band pass filter configurations have been proposed as application examples. The workability of the proposed CDBA and its filter applications have been tested through SPICE simulations by using TSMC 0.25 µm technology. The simulation results depicted that the proposed CDBA provides a very well performance and the results obtained for the filters are in close agreement with theory.

Table 1. Comparison between the proposed CDBA and previously reported works

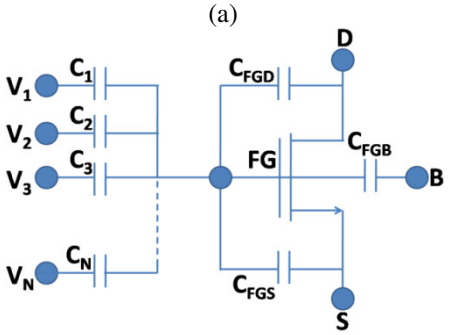
Ref.	Technology (µm)	Supply voltage (V)	No of Transistors	CDBA linear range	CDBA buffer range	Current transfer bandwidth I_z/I_p (MHz)	Current transfer bandwidth I_z/I_n (MHz)	Voltage transfer bandwidth (MHz)
[7]	AD844	± 12	NA	Not reported	Not reported	Not reported	Not reported	Not reported
[14]	0.7	± 1	17	Not reported	Not reported	1000	1000	1000
[15]	Level 3	± 5	45	-3 mA to 3 mA	– 4V to + 4V	70	70	37
[16]	3	± 5	51	Not reported	Not reported	Not reported	Not reported	Not reported
[17]	0.5	± 2.5	20	Not reported	Not reported	Not reported	Not reported	Not reported
[18]	0.5	± 1.25	15	– 30 µA to 30 µA	– 200 mV to + 100 mV	580	643	507
[19]	0.35	± 1.2	18	Not reported	Not reported	Not reported	Not reported	Not reported
[20]	0.18	± 0.6	14	– 60 µA to + 60 µA	– 125 mV to + 75 mV	25	25	474
Proposed CDBA	0.25	± 1.25	21	– 700 µA to + 700 µA	– 1.2 V to + 1V	537	269	502

II. BASICS OF FGMOS TRANSISTOR

FGMOS is a multi-input transistor whose gate is electrically isolated, creating a floating node in DC. A number of secondary gates are deposited above this floating terminal. The secondary gates are capacitively coupled to the floating gate. Threshold voltage of the FGMOS transistor can be tuned by applied bias voltage and capacitor values. The symbol and equivalent representation of an n-type FGMOS with N inputs are shown in Figure 1 [1].



(a)



(b)

Figure 1. (a) Symbol of FGMOS with *N* inputs (b) equivalent circuit of FGMOS

The input voltages $(V_1, V_2, \ldots\ldots, V_N)$ are applied in the gate terminal of FGMOS transistor. The effective voltage on floating gate (V_{FGS}) can be defined as [3]

$$V_{FGS} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{C_{FGD}}{C_T} V_{DS} + \frac{C_{FGB}}{C_T} V_{BS} + \frac{Q_{FG}}{C_T} \quad (1)$$

where C_i(i = 1, 2,…, N) are the capacitors between input gates and the floating gate, V_{DS} is the drain to source voltage and V_{BS} is the substrate to source voltage. Q_{FG} is the amount of residual charge trapped in the floating gate at the time of fabrication.
Total floating gate capacitance can be defined as

$$C_T = \sum_{i=1}^{N} C_i + C_{FGS} + C_{FGD} + C_{FGB} \quad (2)$$

where, C_{FGS}, C_{FGD} and C_{FGB} are parasitic capacitances of floating gate with source, drain and bulk respectively. Assuming $C_i \gg C_{FGS}, C_{FGD}, C_{FGB}$ and Q_{FG} = 0, the drain current I_D of FGMOS transistor in saturation region can be written as [3]

$$I_D = \frac{\beta}{2}\left(\sum_{i=1}^{N} K_i V_{is} - V_T\right)^2 \quad (3)$$

where $K_i = \frac{C_i}{C_T}$, V_{is} is the input gate voltage, V_T is the threshold voltage and β is the transconductance.

III. PROPOSED FGMOS BASED CDBA

CDBA is a four-terminal active block. The block diagram and equivalent circuit of the CDBA are shown in Figure 2, where p is the positive or non-inverting low impedance input port, n is the negative or inverting low impedance input port, w is the low impedance output port and z is the high impedance output port.

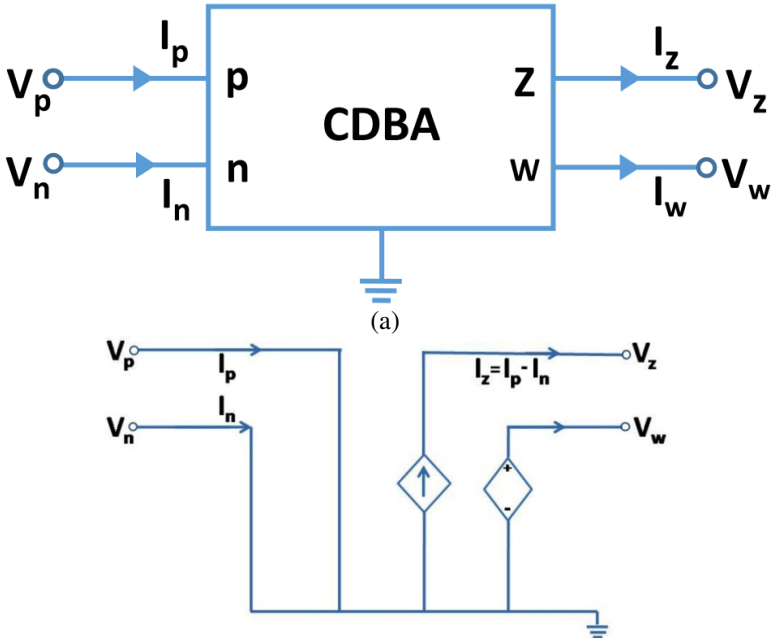


Figure 2. The CDBA (a) circuit symbol and (b) equivalent circuit

The characteristic equation of this block can be defined by the following matrix equations [8]:

$$\begin{bmatrix} V_p \\ V_n \\ V_w \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_w \\ V_z \end{bmatrix} \quad (4)$$

It is clear from the above equation that the current through the z-terminal is equal to the difference of the input currents at the p and n terminals. It is also clear that, the voltage at the w-terminal follows the voltage generated at z-terminal.
The designed CDBA consists of two main blocks: a current subtractor unit of finite input resistances and a voltage buffer unit. Complete schematic of the FGMOS CDBA is shown in Figure 3. The input current subtractor unit is formed by using transistors M1 to M12 [21]. The output buffer unit is formed by using transistors M13 to M19 [2, 3]. In the buffer unit, M13 and M14 are the matched FGMOS transistors. All the MOSFETs and FGMOS transistors are biased to operate in saturation region.

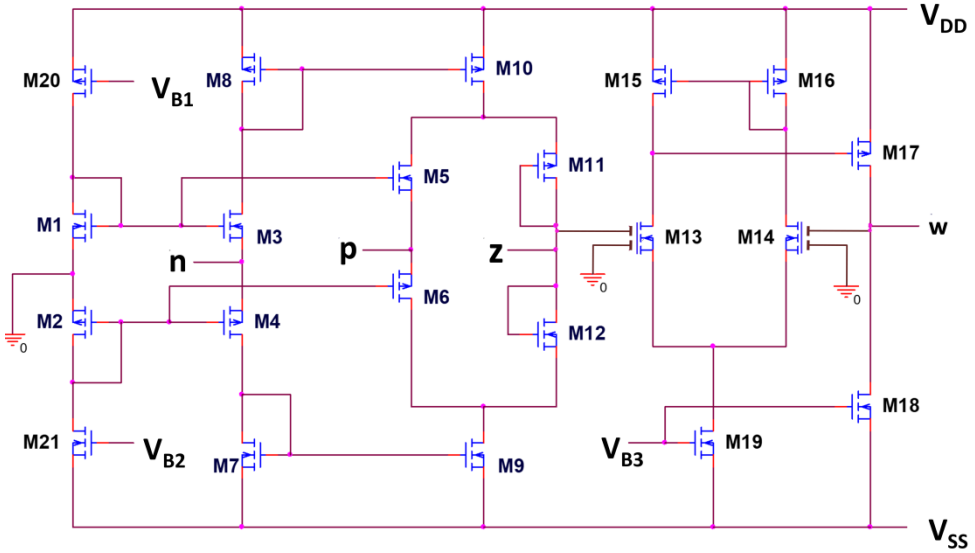


Figure 3. Proposed FGMOS based CDBA

The proposed circuit operates with supply voltages $V_{DD} = -V_{SS} = 1.25$ V. For simulation, TSMC 250 nm technology is used. The value of each FGMOS capacitor is selected as 400 fF. Biasing voltages are set to $V_{B1} = -V_{B2} = 0.7\,V$ and $V_{B3} = -0.45\,V$. Aspect ratios of the transistors are given in Table 2.

Table 2. Aspect ratios of the transistors

Transistor	Aspect Ratio (µm/µm)
M1 – M6	8/1
M7 – M10, M21	5/1
M11, M12, M20	20/2
M13 – M16, M19	5/0.25
M17	100/0.25
M18	50/0.25

Since, the floating gates have no connection with the ground, so during simulation, the simulator reports dc convergence error as it cannot understand the floating gate. The model of the FGMOS transistor proposed in [5] has been used to avoid the issue of dc convergence problem. In this model a large value resistors are connected in parallel with each capacitor to form floating gate inputs as shown in Figure 4. The relation of resistance with capacitance can be expressed as $R_i = 1/kC_i = 10^3$ GΩ where k is known as transconductance parameter and C_i is the value of respective input capacitance.

Figure 5 depicts the DC transfer characteristics of the proposed CDBA. It is evident from Figure 5 that the input linear current range is from – 700 µA to + 700 µA and output linear voltage range is from – 1.2 V to + 1 V.

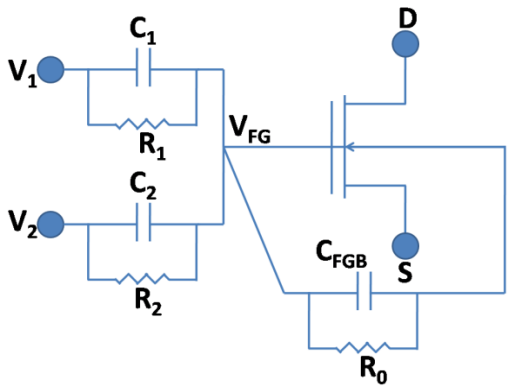
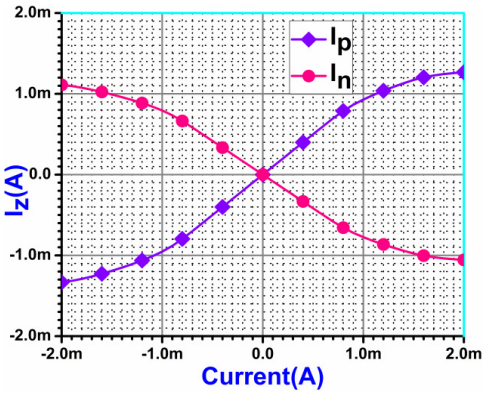


Figure 4. Model of floating gate MOSFET with two inputs [5]



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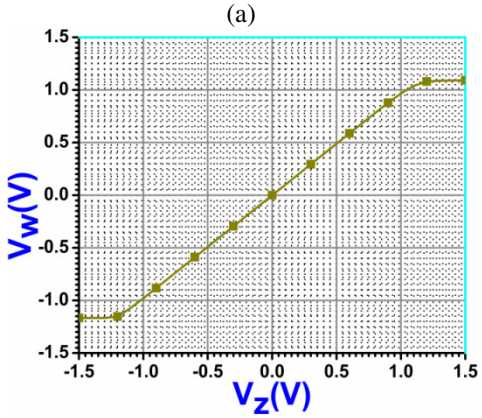

(b)

Figure 5. DC transfer characteristics of FGMOS CDBA: (a) current transfer characteristics (b) voltage transfer characteristic

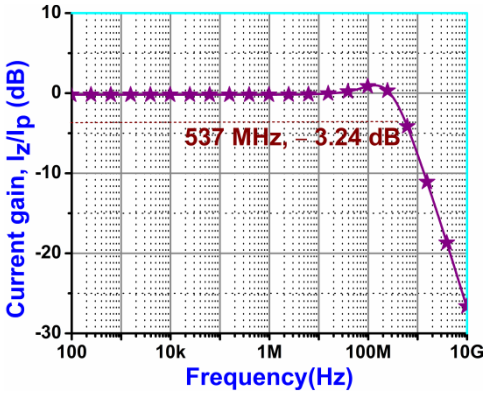

Figure 6. Current gain I_z/I_p

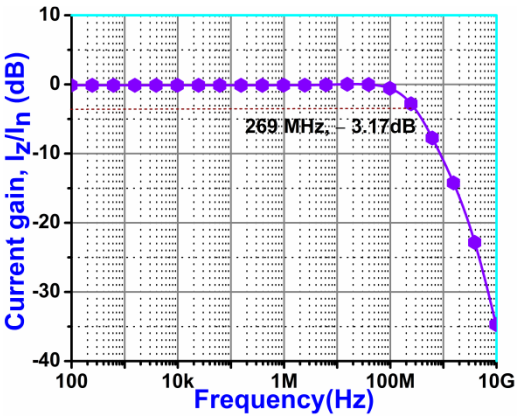

Figure 7. Current gain I_z/I_n

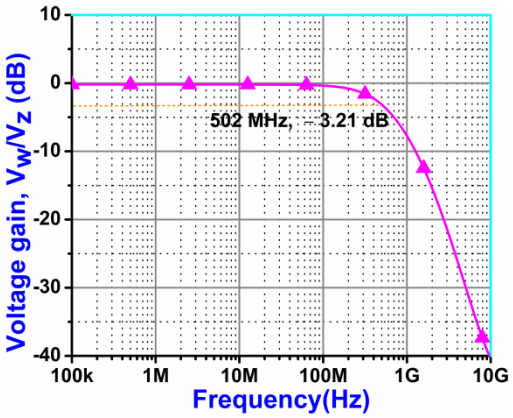

Figure 8. Gain of V_w/V_Z

The current transfer characteristics for I_z/I_p is shown in Figure 6, whereas that for I_z/I_n is depicted in Figure 7. It can be obtained from Figure 6 and Figure 7 that the -3 dB bandwidth of I_z/I_p and I_z/I_n are 537 MHz and 269 MHz respectively. Similarly, the voltage transfer characteristics for V_w/V_Z is illustrated in Figure 8 with the measured bandwidth of 502 MHz. The current and voltage gains, α_p, α_n and β_v are obtained as 0.979, 0.975 and 0.986, respectively. Table 3 shows the summarization of simulation results.

Table 3. Simulated performance of the proposed CDBA

Parameters	Simulation results
Supply voltage(V)	± 1.25
Technology(µm)	0.25
Power Dissipation(mW)	2.78
Current transfer ratio, $\alpha_p = I_z/I_p$	0.979
Current transfer ratio, $\alpha_n = I_z/I_n$	0.975
Voltage transfer ratio, $\beta_v = V_W/V_Z$	0.986
Terminal-p resistance(Ω)	445
Terminal-n resistance(Ω)	524
Terminal-z resistance(kΩ)	822
Terminal-w resistance(Ω)	67
I_z/I_p(– 3 dB bandwidth) (MHz)	537
I_z/I_n(– 3 dB bandwidth) (MHz)	269
V_w/V_z (– 3 dB bandwidth) (MHz)	502
CDBA linear range	– 700 µA to + 700µA
Buffer linear range	– 1.2 V to + 1V

IV. APPLICATIONS OF FGMOS BASED CDBA

The workability of the proposed FGMOS CDBA has been demonstrated through a newly proposed third-order low pass and band pass filter circuits. The proposed circuits have been described in Section IV.1. The non-ideal and sensitivity analysis of the proposed filter circuits have been presented in Sections IV.2. Finally, PSPICE simulation results of the proposed filter circuits have been given in Section IV.3.

IV.1. Proposed Third-Order Low Pass And Band Pass Filter Circuits

Figure 9 shows the schematic diagram of the proposed third-order low pass filter circuit, whereas the same for the proposed third-order band pass filter circuit is given in Figure 10**.** The proposed filter circuits employ one active block (CDBA), three capacitors, four/three resistors for LP/BP response. The expression for voltage transfer function, obtained by the routine circuit analysis, for the proposed low pass filter shown in Figure 9, is given in Equation (5), whereas same for the band pass filter circuit as shown in Figure 10, is given in Equation (6).

$$\left(\frac{V_o}{V_{in}}\right)_{LP} = \frac{\frac{R_2}{R_1}}{D(s)} \qquad (\text{If } R_4 = R_1) \tag{5}$$

$$\left(\frac{V_o}{V_{in}}\right)_{BP} = -\frac{sC_1R_2}{D(s)} \tag{6}$$

where $D(s) = s^3C_1C_2C_3R_1R_2R_3 + s^2\{(C_2R_2 + C_3R_3 - C_3R_2)C_1R_1 + C_2C_3R_2R_3\} + s(C_1R_1 + C_2R_2 + C_3R_3 - C_3R_2) + 1$ (7)

Equation (7) confirms that both the proposed filter circuits are of third-order. The obtained cutoff frequency (ω_0) and quality factor (Q) for both the proposed filters can be expressed as:

$$\omega_0 = \frac{1}{\sqrt[3]{C_1C_2C_3R_1R_2R_3}} \tag{8}$$

$$Q = \frac{\sqrt[3]{C_1C_2C_3R_1R_2R_3}}{C_1R_1 + C_2R_2 + C_3R_3 - C_3R_2 - \sqrt[3]{C_1C_2C_3R_1R_2R_3}} \tag{9}$$

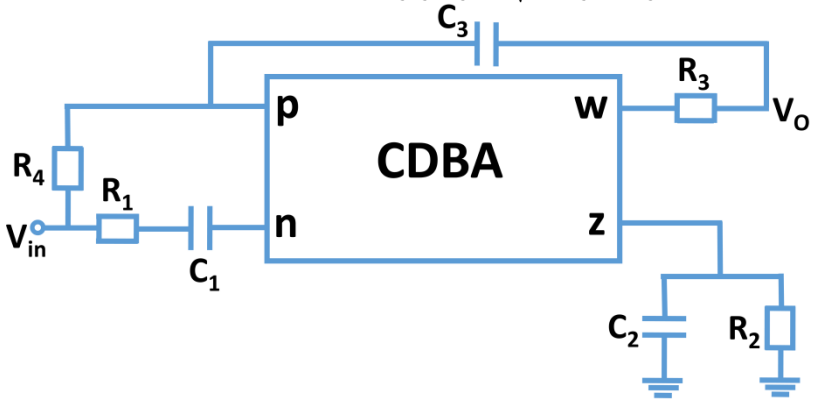

Figure 9. The proposed CDBA based third-order low pass filter circuit

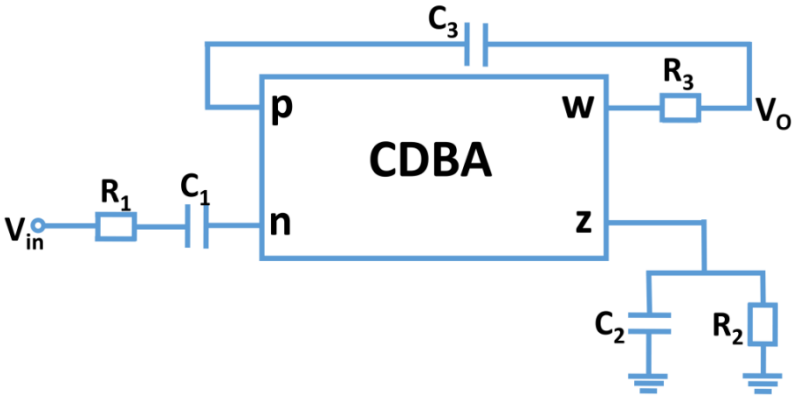

Figure 10. The proposed CDBA based third-order band pass filter circuit

IV.2 Non-Ideal And Sensitivity Analysis Of The Proposed Filters

Current and voltage tracking errors arising from the active element can influence the behavior of the circuit for non-ideal CDBA. So it is necessary to give the effect of the non-idealities on the circuit performance. Including current and voltage tracking error, the port relationship of CDBA can be written as [17]

$$V_p = 0, V_n = 0, I_z = \alpha_p I_p - \alpha_n I_n \text{ and } V_w = \beta V_z \tag{10}$$

where $\alpha_p = (1 - \varepsilon_p)$, $\alpha_n = (1 - \varepsilon_n)$ and $\beta = (1 - \varepsilon_v)$

Here, the terms ε_p ($|\varepsilon_p| \ll 1$), ε_n ($|\varepsilon_n| \ll 1$) are current tracking errors and ε_v ($|\varepsilon_v| \ll 1$)is the voltage tracking error. The modified transfer functions of the low pass and band pass filter can be obtained as

$$\left(\frac{V_o'}{V_{in}}\right)_{LP} = \frac{(\alpha_p + s\alpha_p C_1R_1 - s\alpha_n C_1R_1)\beta\frac{R_2}{R_1}}{D(s)'} \tag{11}$$

$$\left(\frac{V_o'}{V_{in}}\right)_{BP} = -\frac{s\alpha_n\beta C_1R_2}{D(s)'} \tag{12}$$

where $D(s)' = s^3C_1C_2C_3R_1R_2R_3 + s^2\{(C_2R_2 + C_3R_3 - \alpha_p\beta C_3R_2)C_1R_1 + C_2C_3R_2R_3\} + s(C_1R_1 + C_2R_2 + C_3R_3 - \alpha_p\beta C_3R_2) + 1$ (13)

The modified cutoff frequency (ω_0) and quality factor (Q) can be rewritten as

$$\omega_0 = \frac{1}{\sqrt[3]{C_1C_2C_3R_1R_2R_3}} \tag{14}$$

$$Q = \frac{\sqrt[3]{C_1C_2C_3R_1R_2R_3}}{C_1R_1 + C_2R_2 + C_3R_3 - \alpha_p\beta C_3R_2 - \sqrt[3]{C_1C_2C_3R_1R_2R_3}} \tag{15}$$

From the above expression it may concluded that the cutoff frequency is not changed under non-ideal conditions.

The sensitivity of cutoff frequency (ω_0) with respect to passive element can be obtained as

$$S^{\omega_0}_{C_1,C_2,C_3,R_1,R_2,R_3} = -\frac{1}{3} \tag{16}$$

So, equation (15) confirms that the sensitivities of the filters are low and the magnitude is equal to $\frac{1}{3}$. Thus, the sensitivity of the proposed filters is under considerable limits.
From the above discussion it may concluded that the proposed filter circuits can behave excellently even under non-ideal conditions.

IV.3 Simulation Result Of The Proposed Filters

To test the performance of the proposed low pass and band pass filter circuits PSPICE simulation are used. For simulation the value of capacitors are chosen as $C_1 = C_2 = C_3 = 10$ pF. The simulated frequency characteristics for the proposed low pass and band pass filters are shown in Figure 11 and Figure 12, respectively. The value of simulated cutoff frequency of this design is 5.248 MHz when $R_1 = R_2 = R_3 = R_4 = 3$ kΩ. For $R_1 = R_2 = R_3 = R_4 = 1.6$ kΩ the simulated cutoff frequency is found as 9.549 MHz.

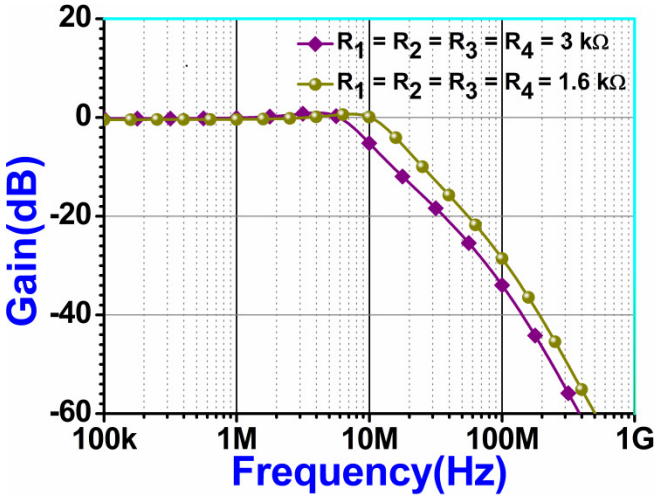

Figure 11. Frequency response of third-order low pass filter

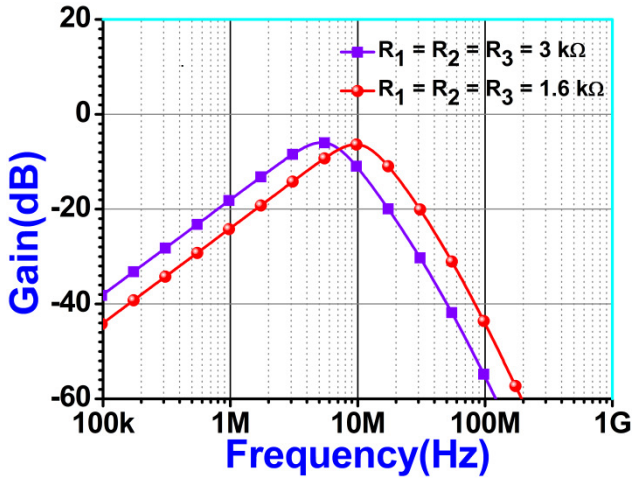

Figure 12. Frequency response of third-order band pass filter

V. CONCLUSIONS

In this paper, FGMOS based high performance CDBA is presented. A wider input linear range for the current inputs and voltage output are achieved. Two applications of the reported FGMOS based CDBA block are reported: such as third order low pass and band pass filter. The filter circuits employ single CDBA, three capacitors, four/three resistors for LP/BP responses. The workability of the proposed CDBA and its applications are verified by PSPICE simulation. Therefore the proposed CDBA and the filters may be beneficial in low voltage analog signal generation applications.

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