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Simulation and Analysis of Symmetric Seven-level CMLI using Multicarrier SPWM Technique with Reducing Number of Switches

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ABSTRACT
This paper presents the simulation and analysis of symmetric seven-level cascaded multilevel inverter (CMLI) using multicarrier sinusoidal pulse width modulation (MC-SPWM) technique with reducing number of switches. The ultimate aim of the paper is, a renewed seven-level inverter topology is introduced incorporating the least number of unidirectional switches and gate trigger circuitry, thereby ensuring the minimum switching losses, reducing size and installation cost. The new proposed topology is well suited for drives and renewable energy applications. The performance quality in terms of total harmonic distortion (THD) and switching losses of the new CMLI is compared with conventional cascaded inverter and other existing seven-level reduced switch topologies using carrier-based pulse width modulation (PWM) techniques. The effectiveness of the proposed system is proved with the help of simulation. The simulation is performed in MATLAB/Simulink. From the simulation results, it shows that the proposed multilevel inverter works properly to generate the multilevel output waveform with minimum number of semiconductor devices and to achieve high dynamic performance with low THD.
Keywords: Multilevel Inverter (MLI), Cascaded Multilevel Inverter (CMLI), Pulse Width Modulation (PWM), Multicarrier Sinusoidal Pulse Width Modulation (MC-SPWM), Total Harmonic Distortion (THD)

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I. INTRODUCTION

Due to environmental problems and lack of fossil fuels, use of renewable energy is increasing day by day. The power electronic converter's cost, power quality, efficiency space and reliability are the main key factor to integrate converter with renewable energy like solar energy, wind energy etc. The term "Multilevel Inverter" (MLI) was rooted years ago. Multilevel inverters offer various applications in voltage ranging from medium to high such as in renewable sources, industrial drives, laminators, blowers, fans, and conveyors. Small voltage step results in making the MLI withstand better voltage, fewer harmonics, high electromagnetic compatibility, reduced switching loss, and better power quality [1-10]. Cascaded multilevel inverters were developed in the initial stage. Later, diode-clamped MLI'S were developed followed by flying capacitor MLI'S. These three topologies utilize different mechanisms to produce the required output. The topology introduced first, that is, the CMLI, is simply series connection of H-bridges. The diode-clamped MLI uses series capacitor bank whereas, in flying capacitor MLI, floating capacitors are used in order to clamp the output voltage. H-bridge inverters have isolation transformers, and then H-bridge cascaded MLI'S were introduced to separate DC input sources. But they do not need either clamping a diode or flying capacitors. Absence of voltage imbalance is the main advantage of cascaded MLI. Fewer components are used in CMLI compared to diode-clamped and flying capacitor MLI [11-18].Most of the researches are carried out in cascaded MLI configuration. But still the new trends are involved in the evolution of renewed multilevel inverters. Modifications are made in its inbuilt structure. To increase the power quality, first three-level multilevel inverter has been reported initially and with the significant changes in the converter topology, MLI can be categorized into three categories (i) symmetrical MLI, (ii) asymmetrical MLI (iii) S-DCMI. The first two types of topologies use more than one DC source and more number of switching devices viz. MOSFET, IGBT etc to increase the number of levels in output voltage. The fifty teen-level multilevel inverter using series and parallel DC sources is used to increase the number of levels by using H-bridge and eleven semiconductor switches [19-29].

A new concept of additive or subtractive combination of different DC sources based multilevel inverter has six unidirectional semiconductor switches and two bidirectional semiconductor switches to generate twenty seven output voltage levels using three DC sources. The demerit of this multilevel inverter is that it constitutes bi-directional semiconductor switches, which further enhance the number of switches, switching and conduction losses in comparison to the unidirectional device. Additionally, a five-level multilevel inverter using addition or subtraction principle of different DC sources is compared with conventional five-level inverter. A symmetrical inverter has been implemented comprising three main parts of an inverter as DC sources, main switches and one H-bridge cell using bidirectional switches [30-45].

The main objective of this inverter has been to reduce the number of switches, losses, installation area and cost with application as dynamic voltage restorer for improving power quality. Asymmetric and symmetric topologies are suggested to reduce the number of switching devices for specified number of output voltage levels. Three algorithms to select magnitude of different DC sources has been reported and implemented on optimal structure MLI. Cascaded cross-switched MLI topology is used as symmetric and asymmetric MLI. To reduce the switching losses, THD and to increase the efficiency a forty seven-level switch ladder MLI topology has been reported. This topology is used a multi winding transformer to create higher number of levels with H-bridge. To reduce the DC sources, cascade hybrid multilevel topology of asymmetric MLI has been reported which uses one H-bridge for each phase with a bottom three leg inverter. An optimal structure has been used to reduce the switches, DC sources, standing voltage and to maximize the number of levels [46-58].

A seven-level MLI was generated with nine switches reducing three switches from the main conventional CMLI. It offers good results yielding desired a seven-level output with low THD. A seven-level MLI with seven switches reducing two more switches from the previous topology made a far improvement in the investigation of the switch reduction. Yet another topology of seven-level MLI was configured with four dc sources and just six switches to get seven-level output. The latter made a drastic move in topology development since the THD is low, and gate circuits used to drive the switches are less [59-65].

It is mentioned everywhere that simplicity is the main advantage of CMLI to generate five-levels using eight switches, seven-levels with twelve switches, nine-levels with sixteen switches, and so on. It clearly reveals that an increase in levels demands more number of switches. Then the comment on simplicity of CMLI is simply contradictory. Hence, the focus was eyeing on a real solution to this problem, that is, how to simplify the complex circuit. Then arise the concept of "switch reduction". Exploring the existing topologies on basic seven-level, switch reduction was made from twelve switches to nine, gradually to seven and then to six.

Aiming at reducing the switches to the maximum possible extent and reducing complexity, the new topology is introduced with five switches for seven-levels, and this would be the least possible reduction. The new MLI configuration is made of five switches eliminating one switch from the existing six switches, seven-level topology in a special arrangement with four inputs DC sources to generate seven-level output. The fewer switches we use lessen the cost of circuit building. The circuit credibility is checked without using PWM. Then identifying the effectiveness in working simulated the circuit with phase disposition (PD), phase opposition disposition (POD), and alternative phase opposition disposition (APOD) using MATLAB/Simulink.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER TOPOLOGY

Using three DC voltage sources, three H-bridge units each with four switches together forming twelve switches in total are used in conventional CMLI which is represented in Fig 1. General expression for output voltage levels, $m= (n+2)/2$ where m is the number of switches in the configuration. Each Bridge is outputting three-levels, $+Vdc, 0, -Vdc$. The three-level CMLI consist of single H-bridge combine with a series of the power conversion cell. Cascaded H-bridge multilevel inverter is better than the diode clamped inverter and flying capacitors inverter, it requires less number of the component in each switching levels.

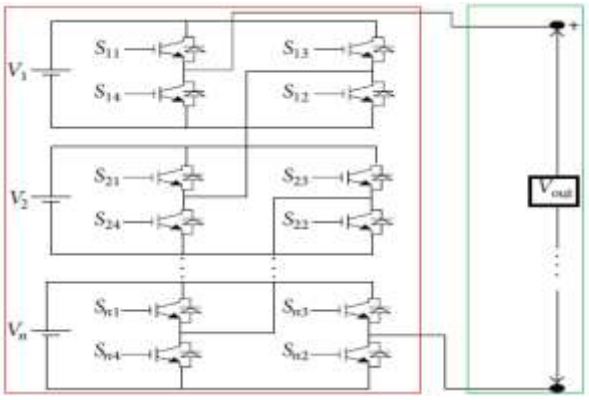

Fig. 1 Conventional cascaded n-level Multilevel Inverter

In cascade H-bridge multilevel inverter, the grouping of switches and capacitors is called H-bridge consisting of isolated DC Voltage source and cascading three Bridges in such a fashion to produce stepped seven-level staircase waveforms. In Existing CMLI Topology, seven-level, nine switches, this topology is built with three dc sources, one H-bridge composed of four switches and then additional five more switches for producing stepped seven-levels, for positive and negative half cycles. In seven-level, seven switches, this topology is made of seven switches and three dc sources. One H-bridge present in the topology is mainly for polarity change. Here, three switches conduct at a time for level generation. In seven-level, six switches, this is a special configuration consisting of four dc sources and six switches. One switch across the load is used for zero level. S_1, S_2, S_3 used for level generation and S_4, S_5 switches for polarity changing.

III. PROPOSED FIVE-SWITCH CMLI TOPOLOGY

The proposed seven-level MLI as shown in Fig 2 is about redesigning of existing six switch topology eliminating one switch attaining the tag of five switch configuration. The circuit thus obtained is the simplest design compared to conventional and all other existing topologies. It consists of four dc sources of seven-levels, for nine-level, five dc sources and so on. Generalized expression for output voltage levels for the new topology proposed is $m = (2\times n-3)$, where m = number of output voltage levels, n = number of switches $m = (2\times V-1)$, where V = number of dc sources.

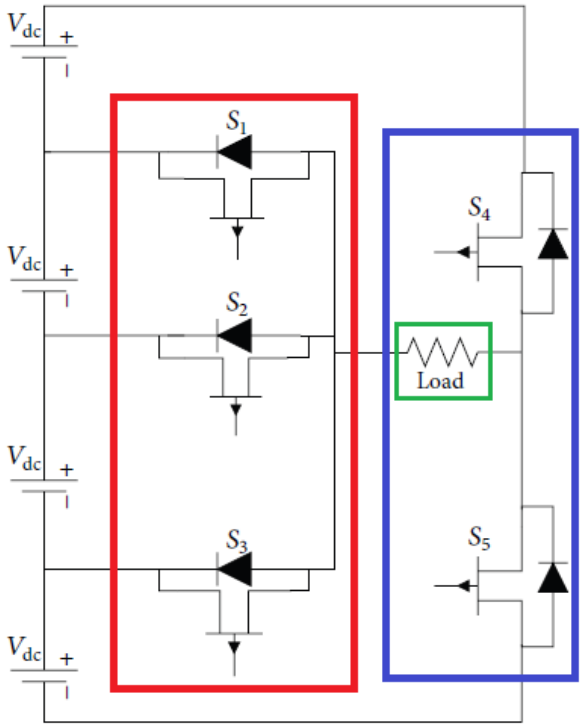

Fig. 2 Seven-level five-switch CMLI topology

The design of pulse generation circuit makes the topology differ from others so as to obtain the unique pulse pattern to trigger the switches at the proper instant. Table 1 represents the switching scheme for the proposed topology. Switches S_1, S_2, and S_3 need to be compulsorily unidirectional or else the output waveform will get distorted. Reduced switches make the circuit compact and user-friendly. The usage of four dc sources for the generation of seven-level MLI results in less utilization of sources, switch reduction benefits in low switching losses. No H-Bridge is used. Just two switches play the role of polarity reversal.

IV. METHODOLOGY AND PULSE GENERATION CIRCUIT

The pulse generation is essential in order to trigger the switches with appropriate pulse pattern to produce the desired seven-level output. It is inevitable to analyze which PWM suits the new topology. The simplest PWM technique is the carrier-based PWM technique. It can be further categorized into level and phase shifting carrier-based PWM, respectively. Since the phase shifting carrier-based PWM yields more harmonics comparatively, the level shifting carrier-based PWM is preferred over it. Therefore, the new circuit design is analyzed with level shifting carrier based PWMs, that is, PD, POD, and APOD PWMs. Interestingly, it is noted that POD gives lower THD and is found to be the apt PWM for proposed topology. The PWM generation circuit is the

heart of the circuitry. One reference sine wave of amplitude 0.8 and frequency 50 Hertz is compared with C_1 to C_6 triangular carriers of frequency 1KHz. If *m*-level needs to be synthesized, *(m-1)* carriers are required. Whenever the reference sinusoid exceeds the carrier, instant pulses are generated to trigger the switch to '*0*' N-state. Higher triangular carrier amplitude is taken as one. The carrier alignment for the carrier based PWM technique is shown in following figures. The pulse waveform of carrier-based PWM techniques with phase disposition (PD)-PWM is shown in Fig 3. The pulse waveform of carrier-based PWM techniques with phase opposition disposition (POD)-PWM is shown in Fig 4.

Table 1 represents the switching scheme for the proposed topology.

S.No	S_1	S_2	S_3	S_4	S_5	*Output Voltage*
1	0	0	1	0	1	*+1Vdc*
2	0	1	0	0	1	*+2Vdc*
3	1	0	0	0	1	*+3Vdc*
4	0	0	0	0	0	*0*
5	1	0	0	1	0	*-1Vdc*
6	0	1	0	1	0	*-2Vdc*
7	0	0	1	1	0	*-3Vdc*

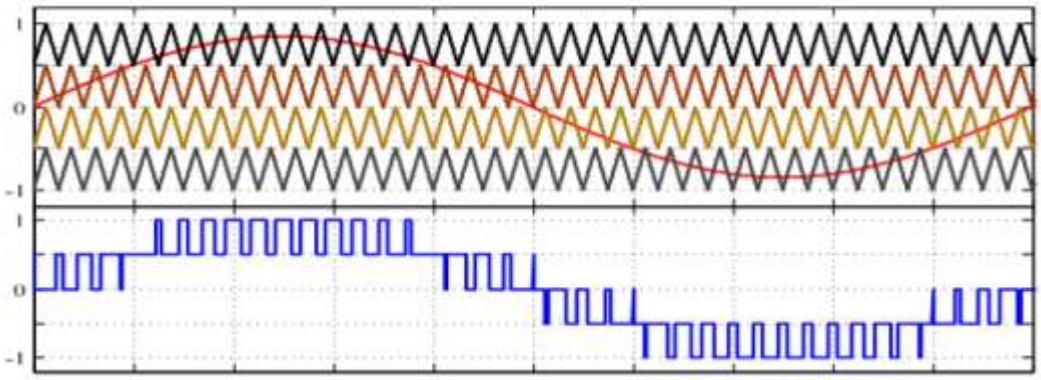

Fig.3 Pulse waveform of carrier-based Phase disposition (PD)-PWM

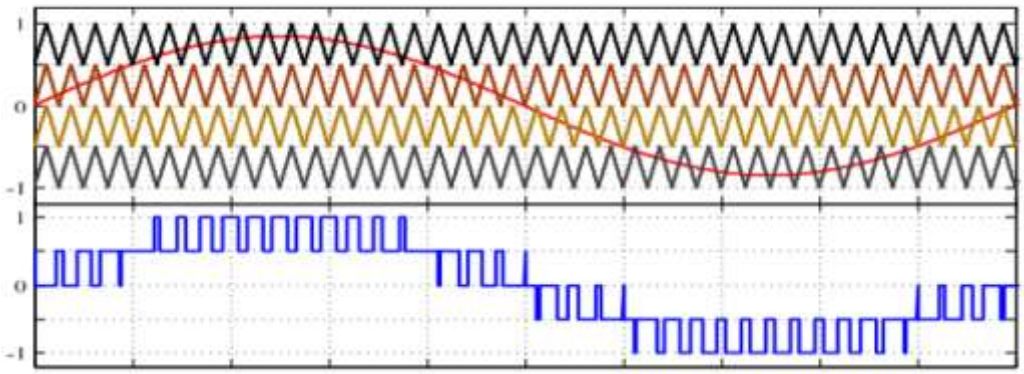

Fig.4 Pulse waveform of carrier-based Phase Opposition Disposition (POD)-PWM

The pulse waveform of carrier-based PWM techniques with alternative phase opposition disposition (APOD)-PWM is shown in Fig 5. In PD or phase disposition technique, *(m-1)* carriers are aligned in the same direction/phase. In POD or phase opposition disposition for seven-level, six carriers are aligned as symmetric mirror images above and below the zero reference axis. In alternate phase opposition disposition, alternate carriers are in the same phase and neighboring carriers in the opposing phase. The reference signal comparing with carrier generating pulse which is then modified feeding to logic gates in order to get the required pattern to trigger the switches at the proper instant. For examples switch S_1 needs to have a pulse so as to obtain *+Vdc* and *−3Vdc* and S_2 require *+2Vdc* and *−2Vdc*. S_3 conducts *+3Vdc* and *−Vdc*. Also, switches S_5 and S_4 conduct positive and negative half cycles, respectively.

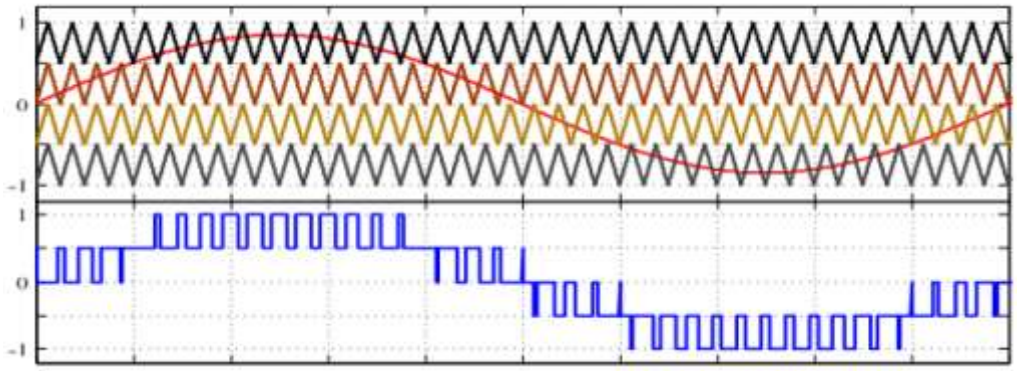

Fig.5 Pulse waveform of carrier-based Alternative Phase Opposition Disposition (APOD)-PWM

V. SIMULATION RESULTS AND DISCUSSION

In the proposed seven-level MLI, the circuit is built of five MOSFET unidirectional switches. It can also be built with three unidirectional and two bidirectional switches. The load is resistive with a value of 10 ohms. Four 10-volt symmetric DC input voltages are used. Note that in order to obtain the shaped seven-level output without distortion, MOSFET block parameters in MATLAB should vary according to the load used. The FFT analysis of seven-level five-switch CMLI using carrier-based Phase disposition (PD)-PWM is shown in Fig 6. The FFT analysis of seven-level five-switch CMLI using carrier-based phase opposition disposition (POD)-PWM is shown in Fig 7. The FFT analysis of seven-level five-switch CMLI using carrier-based alternative phase opposition disposition (APOD)-PWM is shown in Fig 8.

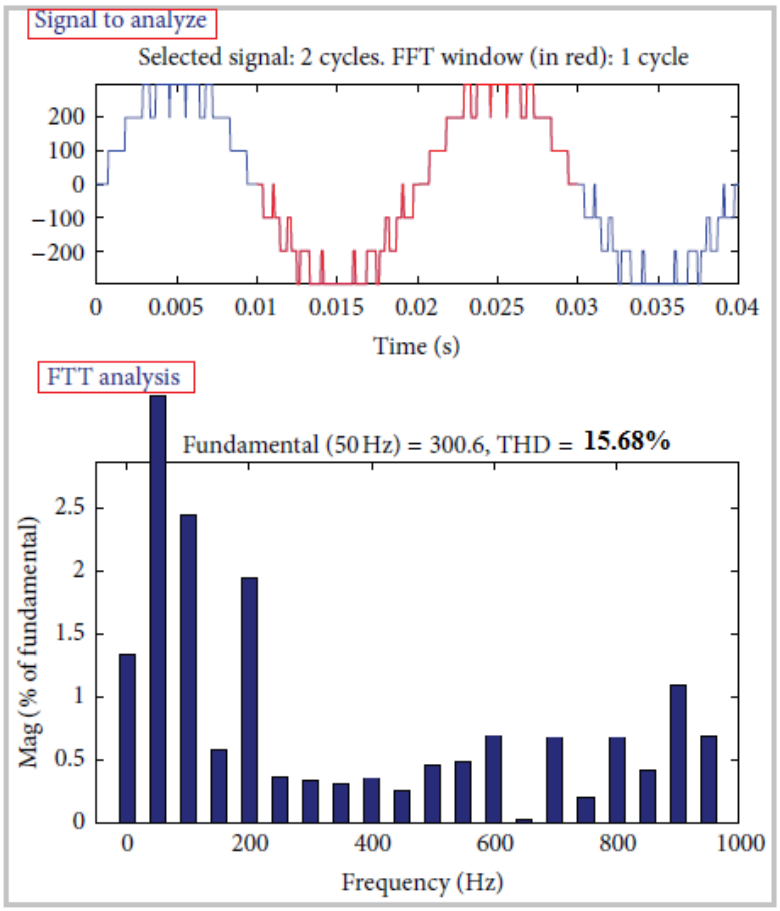

Fig. 6 FFT analysis of seven-level five-switch CMLI using PD PWM.

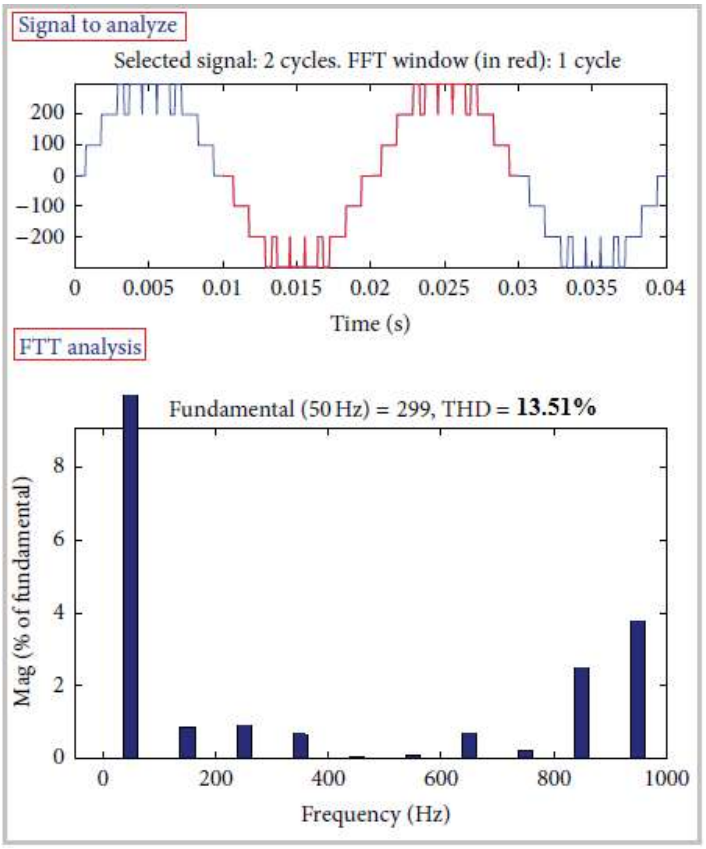

Fig. 7 FFT analysis of seven-level five-switch CMLI using POD PWM.

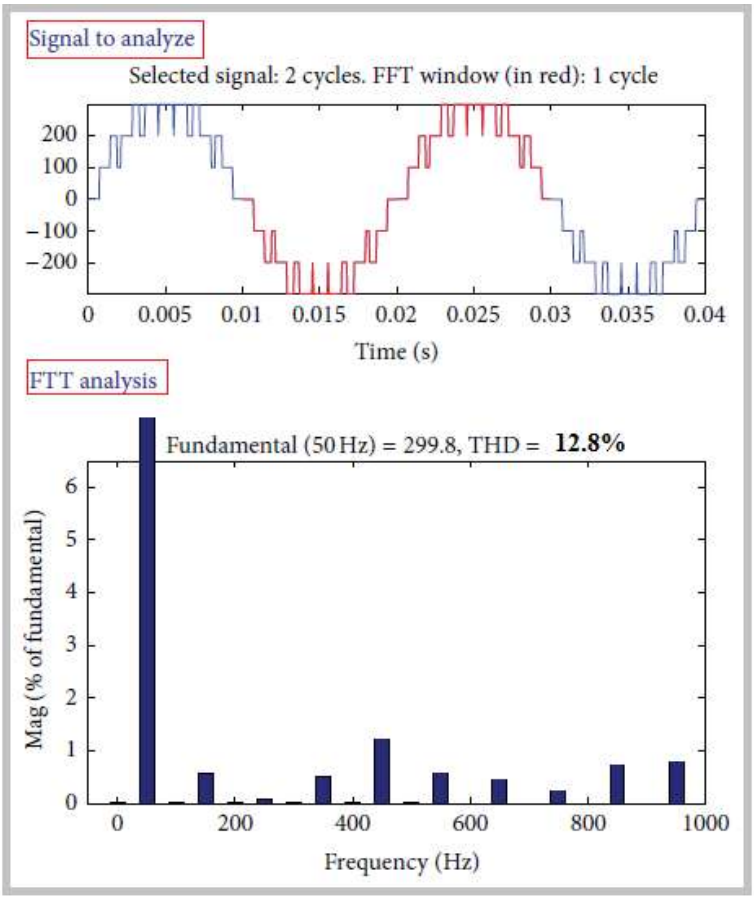

Fig. 8 FFT analysis of seven-level five-switch CMLI using APOD PWM.

VI. CONCLUSION

This paper presents the simulation and analysis of symmetric seven-level cascaded multilevel inverter (CMLI) using multicarrier sinusoidal pulse width modulation (MC-SPWM) technique with reducing number of switches. The seven-level MLI using just five switches is successfully introduced simulating the circuitry using MATLAB/SIMULINK and observed a clear stepped seven-level waveform. It is found that the alternative phase opposition disposition PWM dominates all other PWMs in the proposed configuration. The validity of the proposed method is shown through extensive simulation investigations applied to symmetric seven-level cascaded multilevel inverter.

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