A More Effective Realization Of BCD Adder By Using A New Reversible Logic BBCDC

Shefali Mamataj[1],Biswajit Das[2],Anurima Rahaman[3]
[1] Assistant Professor, Department of ECE Murshidabad College of Engineering &Technology,Berhampore,
[2] Assistant Professor, Department of CSE, Murshidabad College of Engineering &Technology,Berhampore
[3] B.Tech Student, Department of AEIE, Future Institute of Engineering and Management,Sonarpur

Abstract:
Reversible logic is one of the emerging technologies having promising applications in quantum computing nanotechnology, and low power CMOS design. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. With the advent of quantum computer and reversible logic, design and implementation of all devices has received more attention. BCD digit adder is the basic unit of the more precise decimal computer arithmetic. This paper represents a new reversible logic BBCDC and also a more effective realization of BCD adder by using the proposed reversible logic. A comparative result is presented which shows that the proposed design is more effective in terms of number of gates and number of garbage outputs than the existing designs.

KEYWORDS: *Reversible logic, Basic Reversible Gates, BCD adder , Reversible full adder, Constant input, Garbage ,Quantum cost.*

I. INTRODUCTION

In electronics hardware designing energy dissipation is one of the most important factor. Researchers like Landauer have shown that for irreversible logic computations, each bit of information lost, generates kTln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [1]. Bennett showed that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way, since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation [2]. Reversible circuits are those circuits that do not lose information and reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between input and output vectors According to Moore's law the numbers of transistors will double every 18 months. Thus energy conservative devices are the need of the day. The amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those circuits that do not lose information A circuit will be reversible if input vector can be specifically retrieved from output vectors and here is one to one correspondence between input and output [3]. A reversible logic circuit should have the following features [5]:

- Use minimum number of reversible gates.
- Use minimum number of garbage outputs.
- Use minimum constant inputs.

Decimal arithmetic has found promising uses in the financial and commercial applications. This is due to the precise calculations required in these applications as oppose to binary arithmetic where some of decimal fractions can't be represented precisely [16].In the hardware design, binary computing is preferred over decimal computing because of ease in building hardware based on binary number system. In spite of ease in building binary hardware, most of the fractional decimal numbers such as 0.110 cannot be exactly represented in binary, thus their approximate values are used for performing computations in binary hardware. Because the financial, commercial, and Internet-based applications cannot tolerate errors generated by conversion between decimal and binary formats, the decimal arithmetic is receiving significant attention and efforts are being accelerated to build dedicated hardware based on decimal arithmetic [4].

II. BASIC REVERSIBLE LOGIC GATE

2.1.Reversible logic Function:

It is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. The reversible logic circuits must be constructed under two main constraints. They are

- Fan-out is not permitted.
- Loops or feedbacks are not permitted.

In the proposed design these two constraints along with the other parameters are optimized effectively . The important parameters which play a major role in the design of an optimized reversible logic circuit are [17-19] ,

Constants: This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.

Garbage: This refers to the number of outputs which are not used in the synthesis of a given function. These are very essential without which reversibility cannot be achieved.

Gate count: The number of reversible gates used to realize the function.

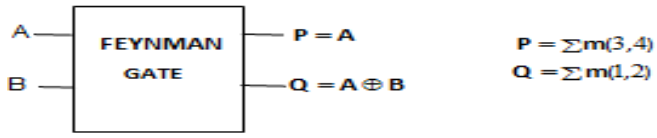
Flexibility: This refers to the universality of a reversible logic gate in realizing more functions.

Quantum cost: This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1X1 or 2X2) required to realize the circuit.

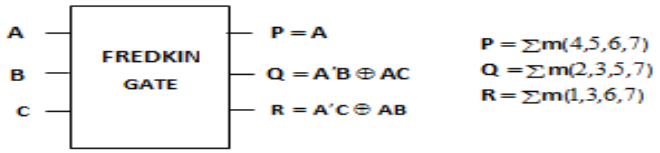
Gate levels: This refers to the number of levels in the circuit which are required to realize the given logic functions.

2.2. Basic Reversible logic Gates

The important basic reversible logic gates are, Feynman gate [6] which is the only 2X2 reversible gate which is as shown in the figure.(1a)and it is used most popularly by the designers for fan-out purposes. There is also a double Feynman gate [7], Fredkin gate [8] and Toffoli gate [9],New Gate[10] , Peres gate[11] , all of which can be used to realize important combinational functions and all are 3X3 reversible gates and are as shown in the figure.(1b) to figure.(1e) .The figures also shows the switching functions for terminals.



Figure(1a) Feynman gate – 2X2 gate



Figure(1b) Fredkin gate – 3X3 gate

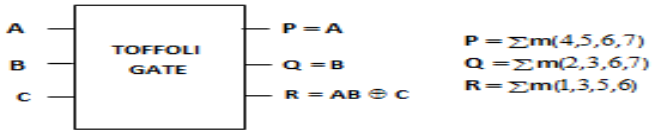


Figure.(1c) Toffoli gate – 3X 3 gate

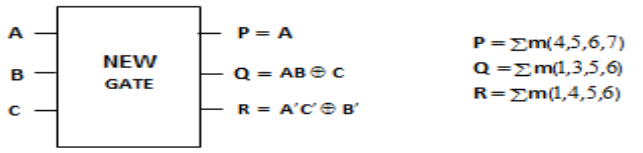
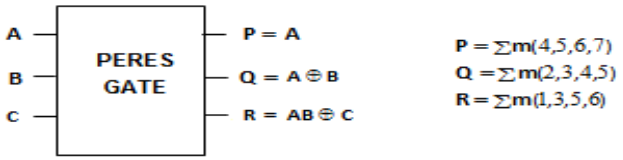
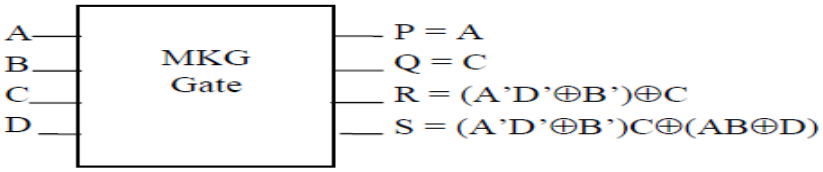


Figure.(1d) New gate – 3X 3 gate

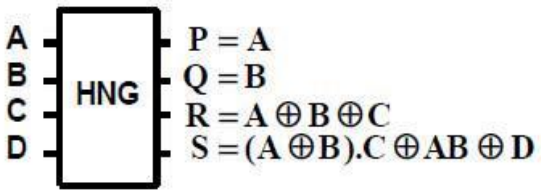


Figure(1e) Peres gate – 3X 3 gate

There are other 4X4 gates some of which are specially designed for the realization of important combinational circuit functions in addition to some basic functions. Some of the important 4X4 gates are, TSG gate [13],MKG gate [12],HNG gate [14]etc, shown in figure(2a,2b,2c) all of which are very useful for the construction of important reversible adders.



Figure(2a) Block diagram of MKG Gate



Figure(2b) Block diagram of HNG Gate diagram

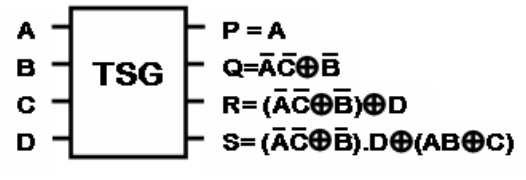
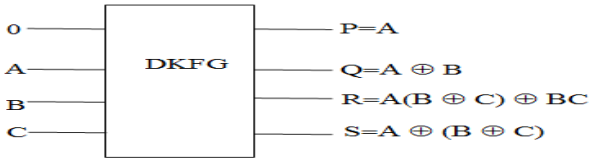


Figure (2c): TSG Gate Block

2.3.Reversible logic DKFG gate

A 4X4 reversible gate DKFG already had been proposed [20] shown in figure 2. In this gate the input vector is given by I_V=(0,A,*B*,C) and the corresponding output vector is O_V=(*P*,*Q*,*R*,*S*).



. Figure(3a): DKFG reversible gate

We can use DKFG gate as a full-adder as shown in fig3b

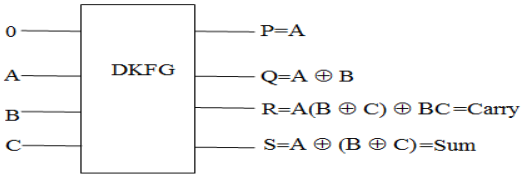


Figure (3b): DKFG gate implemented as Full adder

III. PROPOSED 5 X 5 REVERSIBLE GATE

A 5X5 reversible gate BBCDC (Binary to BCD conversion) logic has been proposed in this paper (See Figure 4) for BCD adder circuit application. The Truth table for the corresponding gate is shown in TABLE I . A closer look at the Truth Table reveals that the input pattern corresponding to a specific output pattern can be uniquely determined and thereby maintaining that there is a one-to-one correspondence between the input vector and the output vector. In this gate the input vector is given by *IV*=(A,*B*,C,D,E) and the corresponding output vector is*OV*=(*P*,*Q*,*R*,*S*,T)

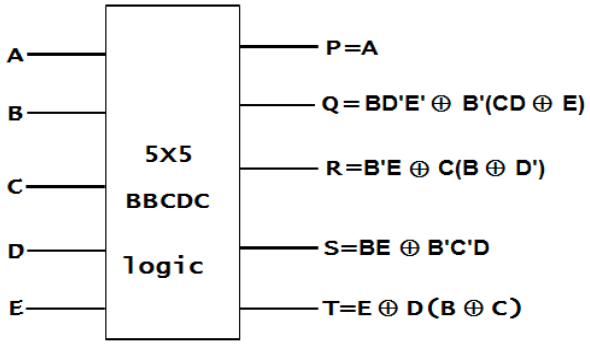


Figure 4: BBCDC reversible gate

TABLE I TRUTH TABLE OF BBCDC

INPUTS					OUTPUTS				
E	D	C	B	A	T	S	R	Q	P
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	0	1	1
0	0	1	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1	0	1
0	0	1	1	0	0	0	1	1	0
0	0	1	1	1	0	0	1	1	1
0	1	0	0	0	0	1	0	0	0
0	1	0	0	1	0	1	0	0	1
0	1	0	1	0	1	0	0	0	0
0	1	0	1	1	1	0	0	0	1
0	1	1	0	0	1	0	0	1	0
0	1	1	0	1	1	0	0	1	1
0	1	1	1	0	1	0	1	0	0
0	1	1	1	1	1	0	1	0	1
1	0	0	0	0	1	0	1	1	0
1	0	0	0	1	1	0	1	1	1
1	0	0	1	0	1	1	0	0	0
1	0	0	1	1	1	1	0	0	1

IV. CONVENTIONAL BCD ADDER CIRCUIT

A Binary Coded Decimal (BCD) adder is a circuit which adds two 4-bit BCD numbers in parallel and produces a 4-bit BCD result. Fig. 5 shows the block diagram of conventional BCD adder. The circuit must include the correction logic to produce valid BCD output. Two 4-bit BCD numbers A($A_3A_2A_1A_0$) and B($B_3B_2B_1B_0$) along with carry input is added using conventional 4-bit parallel adder, 4-bit sum and a carry is taken out. If the carry output is set or if the result is greater than nine, binary 0110 is added to the intermediate sum output with the help of second stage 4-bit parallel adder circuit shown in figure5. In a BCD adder, the correction logic which generates the C_{out} is given by, $C_{out} = S_3S_2 + S_3S_1 + C_4$

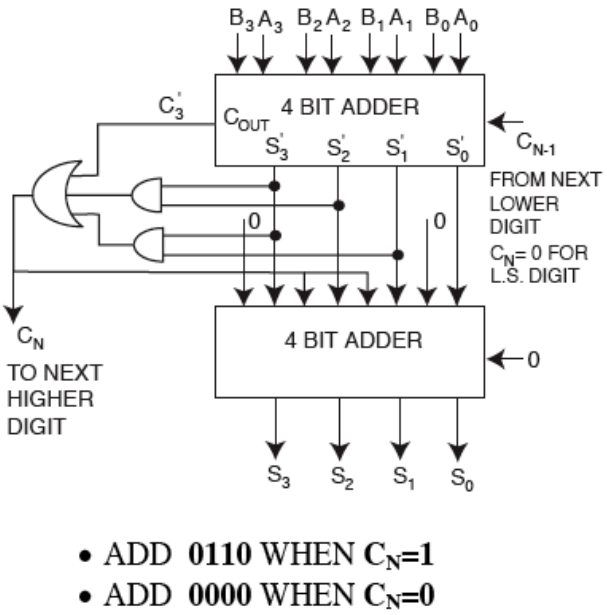


Figure 5: Conventional BCD adder circuit

V. PROPOSED BCD ADDER CIRCUIT

A BCD adder can be realized by using two parts, first part represents a four bit parallel adder and the second part gives us the appropriate addition result in the form of BCD number. The 4-bit parallel adder can be constructed using HNG gates or DKG gates or TSG gates or MKG gates. But we have designed the adder circuit by using DKFG reversible gate as a full adder. The proposed BCD adder circuit is shown in figure 6. Here two BCD numbers A($A_3A_2A_1A_0$) and B ($B_3B_2B_1B_0$) are to be added and we got the result of the BCD addition as S'_3 S'_2 S'_1 S'_0 and final carry output K from the adder circuit. The minimum value of the one bit BCD addition is 0(0000) and the maximum value should be 19(10011).

The BCD sum cannot be greater than 19 because the range of a one bit BCD number is 0-9.Now if carry =1,then the maximum BCD sum will be 9+9+1=19.So in our proposed circuit we will get the maximum BCD sum (19) in binary form as $S'_3=0$, $S'_2=0$, $S'_1=1$, $S'_0=1$ and K=1 .But this is not the correct BCD form .We will get the result in binary form(10011).So for getting the corrected form of BCD sum we have to convert this binary sum into BCD form by using appropriate logic. So for this we have used here a new BBCDC logic for this conversion. If we follow the truth table of BBCDC ,we can see that we can get the appropriate BCD form11001 instead of 10011 .So here $S_3S_2S_1S_0$ is the corrected form of BCD sum and the minimum value is $C_{out}S_3S_2S_1S_0$=00000 and the maximum value will be $C_{out}S_3S_2S_1S_0$= 11001 which is the appropriate form of BCD sum.

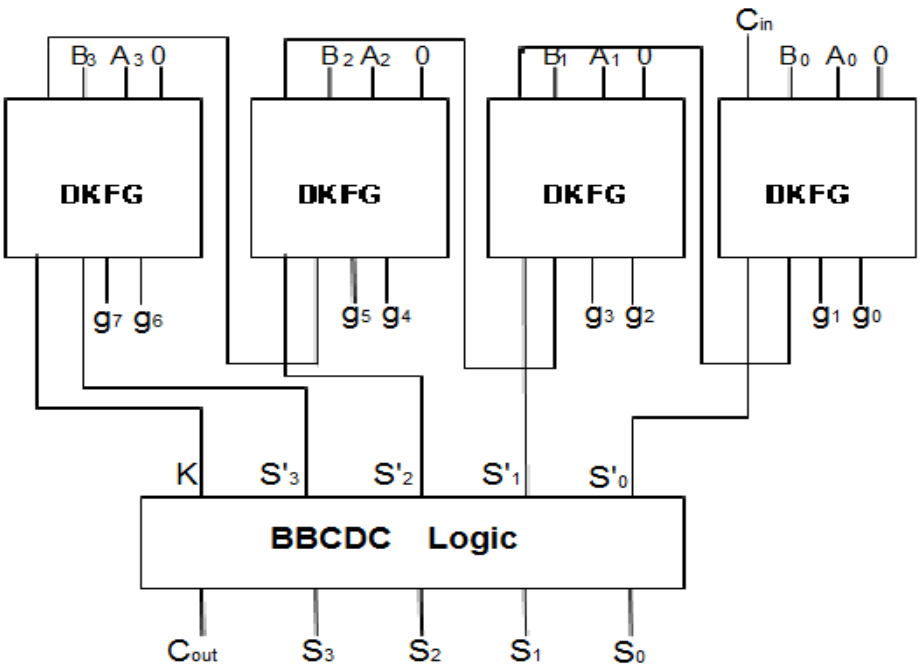


Figure 6: Proposed BCD adder circuit

TABLE III COMPARISON OF EXISTING BCD ADDERS AND PROPOSED BCD ADDER

Name of circuit	I. Different parameters		
	No. of Garbage output	No. of Constant input	No. of reversible gates
BCD adder[21]	22	17	23
BCD adder[22]	22	17	14
BCD adder[23]	22	11	11
BCD adder[24]	11	7	10
BCD adder[25]	10	6	8
BCD adder[26]	11	7	9
PROPOSED BCD adder	8	8	5

.

VI. CONCLUSION

We have realized BCD adder circuit by using DKFG and BBCDC reversible gates and made comparisons in TABLE II. The analysis of various implementations discussed is tabulated in TABLE II. It gives the comparisons of the different designs in terms of the important design parameters like number of reversible gates, number of garbage outputs, and number of constant inputs parameter. From the table it is observed that the present proposal uses least number of gates producing least number of garbage outputs. The efficient design of the BCD adder depends on the design methodology used for designing the reversible ripple carry adder and the reversible binary to BCD converter. Thus for future research, efficient design schemes for reversible ripple carry adder and the reversible binary to BCD converter is an interesting area to investigate. Alternate optimization methods are under investigation as a future work.

REFERENCES

[1] R. Landauer, -Irreversibility and Heat Generation in the computational Process, IBM Journal of Research and Development, 5, pp. 183-191, 1961.

[2] C.H. Bennett, Logical Reversibility of Computation‖, IBM J.Research and Development, pp. 525-532, November 1973.

[3] Pradeep singla and Naveen kr. Malik " A Cost - Effective Design of Reversible programmable logic array" International Journal Of Computer Application , volume 41 – no. 15, march- 2012.

[4] L. Wang, M. Erle, C. Tsen, E. M. Schwarz, and M. J.Schulte, "A survey of hardware designs for decimal arithmetic," IBM J. Research and Development, vol. 54, no. 2, pp. 8:1 – 8:15, 2010.

[5] Perkowski, M. and P. Kerntopf, "Reversible Logic. Invited tutorial", Proc. EURO-MICRO, Sept 2001, Warsaw, Poland.

[6] R. Feynman, "Quantum Mechanical Computers",Optical News,1985, pp. 11-20.

[7] B. Parhami; "Fault Tolerant Reversible Circuits" Proc. 40th Asilomar Conf. Signals, Systems, and Computers, Pacific Grove,CA, Oct.2006.

[8] E. Fredkin, T. Toffoli, "Conservative Logic",International Journal of Theor. Physics, 21, 1982, pp.219-253.

[9] T. Toffoli., "Reversible Computing", Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science (1980).

[10] Md. M. H Azad Khan, "Design of Full-adder With Reversible Gates", International Conference on Computerand Information Technology,Dhaka, Bangladesh, 2002,pp.515-519.

[11] Peres, A., 1985. Reversible logic and quantum computers, Physical Review: A, 32 (6): 3266-3276.

[12] Haghparast, M. and K. Navi, 2007. A Novel Reversible Full Adder Circuit for Nanotechnology Based Systems. J. Applied Sci., 7 (24): 3995-4000.

[13] Thapliyal H., S. Kotiyal, M. B. Srinivas, 2006.Novel BCD adders and their reversible logic implementation for IEEE 754r format. Proceedings of the 19th International Conference on VLSI Design, 3-7 Jan 2006.

[14] Haghparast M. and K. Navi, 2008. A Novel reversible BCD adder for nanotechnology based systems. Am. J. Applied Sci., 5(3): 282-288.

[15] "Optimal design of a reversible full adder" in International Journal of unconventional computing by Yvan Van Rentergen and Alexis De Vos.

[16] Cowlishaw, M.F., 2003. Decimal Floating-Point:Algorism for Computers. Proceedings of the 16th IEEE Symposium on Computer Arithmetic,pp: 104-111.

[17]. Kerntopf, P., M.A. Perkowski and M.H.A.Khan, 2004. On universality of general reversible multiple valued logic gates, IEEE proceeding of the 34th international symposium on multiple valued logic (ISMVL'04), pp: 68-73.

[18] . Perkowski, M., A. Al-Rabadi, P. Kerntopf,A.Buller, M.Chrzanowska -Jeske, A.Mishchenko, M.Azad Khan, A. Coppola,S.Yanushkevich, V.Shmerko and L. Jozwiak,2001." A general decomposition for reversible logic", Proc.RM'2001, Starkville, pp:119-138.

[19] Perkowski, M. and P. Kerntopf, 2001.Reversible Logic.Invitedtutorial, Proc.EURO- MICRO, Sept 2001, Warsaw, Poland.

[20] An Approach for Realization of 2's Complement Adder Subtractor Using DKG Reversible gate '' Shefali Mamataj, Biswajit Das, Anurima Rahaman" International Journal of Emerging Technology and Advanced Engineering", Vol-3, Issue 12, December 2013.

[21] Hafiz Md. Hasan Babu and A. R. Chowdhury, Design of a Reversible Binary Coded Decimal Adder by Using Reversible 4-bit Parallel adder", VLSI Design 2005, pp-255-260, Kolkata, India,January 2005.

[22] M. Haghparast and K. Navi, 2008. A Novel reversible BCD adder for nanotechnology based systems. Am. J. Applied Sci., 5(3): 282-288.

[23] Thapliyal H., S. Kotiyal, M. B. Srinivas, 2006.Novel BCD adders and their reversible logic implementation for IEEE 754r format. Proceedings of the 19th International Conference on VLSI Design, 7Jan 2006 .

[24] K.Biswas,et.al., "Efficient approaches for designingreversible Binary Coded Decimal adders'' Microelectron, J(2008)doi 10.10.16/j.mejo.2008.04.003

[25] H R Bhagyalakshmi,M K Venkatesh "Optimized reversible BCD adder using new reversible logic gates"journal of computing Vol- 2, Issue- 2, February 2010.

[26] James.R.K; Shahana, T.K.; Jacob, K.P.; Sasi, S. "A New Look at Reversible Logic Implementation of Decimal Adder", System on-Chip,2007, The International Symposium on System-on-Chip Tampere, Finland Nov 20-22, 2007 Year 2007.