

Wi MAX Deinterleaver's Address Generation Unit through FPGA Implementation

Rasika Kulkarni¹, Prof.Priti Rajput²,Prof. Sandeep K. Shelke³

¹ Second Year ME, Signal Processing, DYPSOEA, Ambi

² Prof, DYPSOEA, Ambi ³Prof,DYPSOEA,Ambi

ABSTRACT

The IEEE 802.16 standard, commonly known as WiMAX has broadband wireless access over long distance. WiMAX has evolved from 802.16 to 802.16d for fixed wireless access and IEEE 802.16e standard is for mobility support. WiMAX Forum created the name "WiMAX". The forum describes WiMAX as "a standards-based technology enabling the delivery of last mile wireless broadband access as an alternative to cable and DSL". WiMAX is similar to Wi-Fi, but it can enable usage at much larger scale and at faster speeds [1]. In order to minimize the effect of burst error, the channel interleaver/deinterleaver employed in the WiMAX transceiver is used. The channel interleaver/deinterleaver consists of two memory blocks and an address generator. The objective of this project is to implement an area and delay efficient circuitry for address generator for WiMAX 2-D Deinterleaver using the Xilinx FPGA for all permissible code rates and modulation schemes. This project also build up a generalized circuit for all permissible Ncbps without manual computation of column number.

Keywords: Digital circuits, error correction, field programmable gate arrays (FPGAs), wireless systems.

I. INTRODUCTION

1. Introduction

BROADBAND wireless access (BWA) is continuously becoming a more challenging competitor to the conventional wired last mile access technologies [1]. IEEE has developed standards for mobile BWA (IEEE 802.16e) popularly referred to as mobile WiMAX [2]. The channel interleaver employed in the WiMAX transceiver plays a vital role in minimizing the effect of burst error.

In this brief, a novel, low-complexity, high-speed, and resource-efficient address generator for the channel deinterleaver used in the WiMAX transceiver eliminating the requirement of floor function is proposed. Very few works related to hardware implementation of the interleaver/deinterleaver used in a WiMAX system is available in the literature. The work in [3] demonstrates the grouping of incoming data streams into the block to reduce the frequency of memory access in a deinterleaver using a conventional look-up table (LUT)- based CMOS address generator for WiMAX. Khater *et al.* [4] has described a hardware description language (VHDL)-based implementation of address generator for IEEE 802.16e channel interleaver with only a 1/2 code rate. In [5], the authors have described a finite-state machine (FSM)-based address generator of the same interleaver for all permissible code rates and modulation schemes. Both [4] and [5] are tested on the field-programmable gate array (FPGA) platform

II. TYPES OF WIMAX

There are two types of usage models for WiMAX family of standards - fixed usage model and mobile usage model. The difference between these two systems is the ground speed at which the systems are designed to manage. Wireless access can be divided into 3 classes : stationary, pedestrian and vehicular. The stationary and pedestrian classes are served by the fixed wireless access system and mobile wireless access system address the vehicular class.

III. FIXED WIMAX

Fixed WiMAX is used to refer to systems built using 802.16-2004 (802.16) and the OFDM PHY as the air interface technology. Fixed WiMAX offers cost effective point to point and point to multipoint solutions. WiMAX provides fixed, portable or mobile non-line-of sight service from a base station to a subscriber station, known as customer premise equipment (CPE).

V. WIMAX MODEL

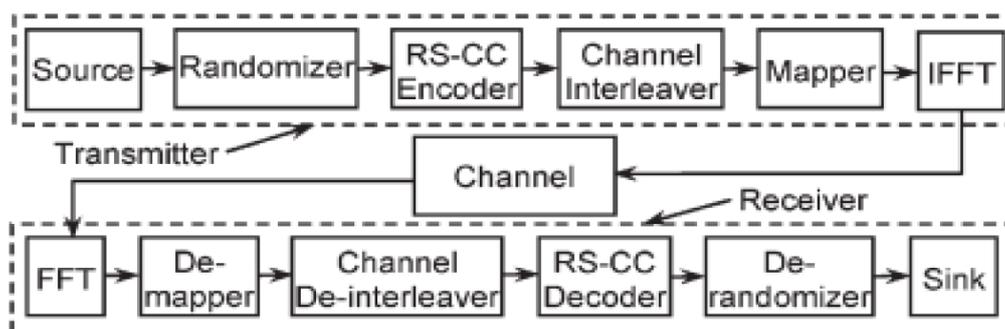


Figure 3: Block diagram of the WiMAX transceiver.

Hardware implementation of floor function is very complex and consumes abnormally large amount of resources [6]. Conventional LUT-based technique is found to be unattractive from many aspects such as slowness in operation, consumption of large logic resources leading to inefficiency in resource utilization, etc. A comparative study with a LUT-based technique confirms the superiority of our proposed design. As compared with the complicated and lengthy expressions, particularly for 16-QAM and 64-QAM, due to the 2-D translation in [6], a compact and user-friendly mathematical representation and subsequent algorithm is proposed. The mathematical expressions have formally been proven using [6]. Our proposed algorithm when realized by digital hardware results in low-complexity architecture for the address generator compared with prevailing technique. A detailed view of the proposed hardware compared with [6] is presented. To make the design compact, the authors adopted optimization by sharing the common hardware between the modules for quadrature phase-shift keying (QPSK), 16-QAM, and 64-QAM. This architecture is modeled in VHDL and implemented on the Xilinx Spartan-3 FPGA.

VI. INTERLEAVER/ DEINTERLEAVER

Interleaving is a process to make a system more efficient, fast and reliable by arranging data in a noncontiguous manner. Interleaving divides memory into small chunks. It is used as a high-level technique to solve memory issues for motherboards and chips. By increasing the bandwidth, the overall performance of the processor and the system increases. This is because the processor can fetch and send more data to and from memory in the same amount of time. Interleaving is the only technique supported by all kinds of motherboards. High-level processing management systems are constantly required to implement such techniques.

VII. CONCLUSION

WiMAX Transceiver is a system which is used for transmission and reception of wireless data in the WiMAX technology. A detailed literature survey is carried out on WiMAX deinterleaver address generator.

A design along with its mathematical formulation for address generation circuitry of the WiMAX transceiver deinterleaver is presented. It supports all permitted code rates and modulation schemes as per IEEE 802.16e. The design is coded using Verilog HDL. Simulation and synthesis is carried out using Xilinx ISE Sim. The simulation results for QPSK, 16-QAM and 64-QAM for all Ncbps values are presented.

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