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Area-Delay Efficient Binary Adders in QCA

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ABSTRACT:
As transistors decrease in size more and more of them can be accommodated in a single die, thus increasing chip computational capabilities. However, transistors cannot get much smaller than their current size. The quantum-dot cellular automata (QCA) approach represents one of the possible solutions in overcoming this physical limit, even though the design of logic modules in QCA is not always straightforward. In this brief, we propose a new adder that outperforms all state-of-the art competitors and achieves the best area-delay tradeoff.

The above advantages are obtained by using an overall area similar to the cheaper designs known in literature. The 64-bit version of the novel adder spans over 18.72 μm2 of active area and shows a delay of only nine clock cycles, that is just 36 clock phases.

KEYWORDS -*Verilog HDL, Xilinx 14.3.*

I. INTRODUCTION

Quantum-dot cellular automata (QCA) are an attractive emerging technology suitable for the development of ultra dense low-power high-performance digital circuits. Quantum-dot cellular automata (QCA) which employs array of coupled quantum dots to implement Boolean logic function. The advantage of QCA lies in the extremely high packing densities possible due to the small size of the dots, the simplified interconnection, and the extremely low power delay product. A basic QCA cell consists of four quantum dots in a square array coupled by tunnel barriers. Electrons are able to tunnel between the dots, but cannot leave the cell. If two excess electrons are placed in the cell, Coulomb repulsion will force the electrons to dots on opposite corners. There are thus two energetically equivalent ground state polarizations can be labeled logic "0"and "1".The basic building blocks of the QCA architecture are AND,OR and NOT. By using the Majority gate we can reduce the amount of delay.i.e by calculating the propagation and generational carries.

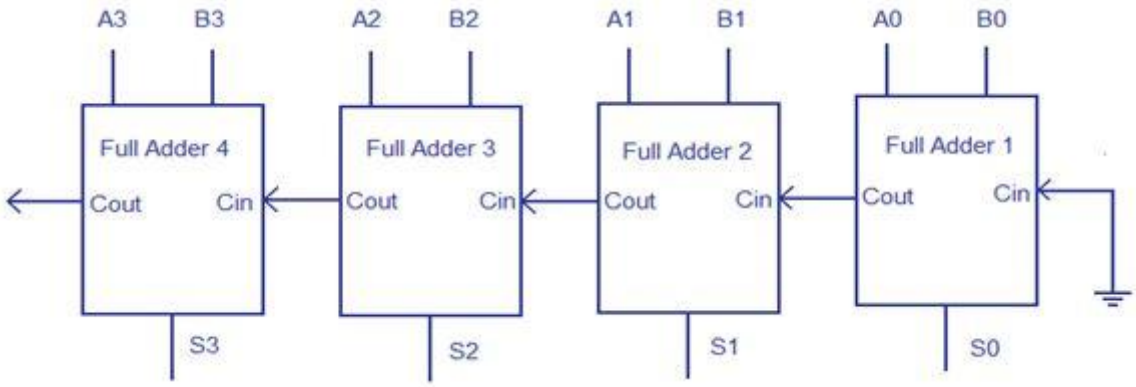
II. REGULAR METHOD

A. Description

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N-bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output.

Consider a NOT gate, When the input is "0″ the output will be "1″ and vice versa. The time taken for the NOT gate's output to become "0″ after the application of logic "1″ to the NOT gate's input is the propagation delay here. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal and the occurrence of the carry out (Cout) signal.

B. *RCA architecture*



C. Basic Full adder block

To understand the working of a ripple carry adder completely, you need to have a look at the full adder too. Full adder is a logic circuit that adds two input operand bits plus a Carry in bit and outputs a Carry out bit and a sum bit.. The Sum out (Sout) of a full adder is the XOR of input operand bits A, B and the Carry in (Cin)bit. Truth table and schematic of a 1 bit Full adder is shown below

There is a simple trick to find results of a full adder. Consider the second last row of the truth table, here the operands are 1, 1, 0 ie (A, B, Cin). Add them together ie 1+1+0 = 10 . In binary system, the number order is 0, 1, 10, 11……. and so the result of 1+1+0 is 10 just like we get 1+1+0 =2 in decimal system. 2 in the decimal system correspond to 10 in the binary system. Swapping the result "10″ will give S=0 and Cout = 1 and the second last row is justified.

Inputs			Outputs	
A	B	Cin	Cout	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

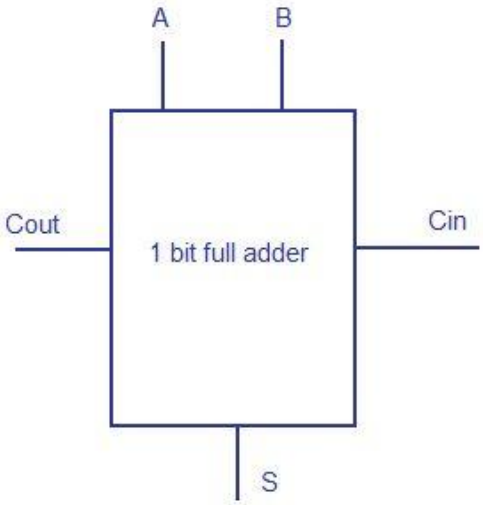


Fig ; 1 bit full adder schematic and truth table

III. PROPOSED METHOD

A.Description

Quantum Dot Cellular Automata (sometimes referred to simply as quantum cellular automata, or QCA) are proposed models of quantum computation, which have been devised in analogy to conventional models of cellular automata introduced by von Neumann. Standard solid state QCA cell design considers the distance between quantum dots to be about 20 nm, and a distance between cells of about 60 nm. Just like any CA, Quantum (-dot) Cellular Automata are based on the simple interaction rules between cells placed on a grid. A QCA cell is constructed from four quantum dots arranged in a square pattern. These quantum dots are sites electrons can occupy by tunneling to them.

B. Cell Design

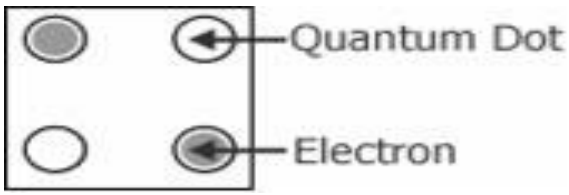


Fig: Simplified Diagram of QCA Cell

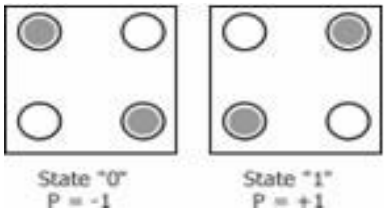


Fig :Four Dot Quantum Cell

C. Structure of Majority gate

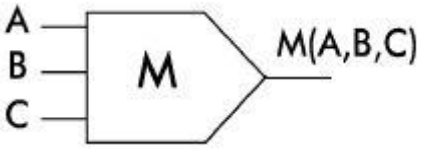


Fig: Structure of Majority gate

D. QCA Majority Gate:

The QCA majority gate performs a three-input logic function. Assuming the inputs are A ,B and C, the logic function of the majority gate is

$$M = AB+BC+CA$$

E. Architecture of Basic Novel 2-bit adder

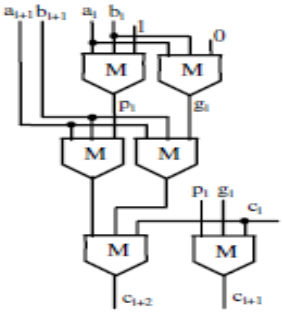
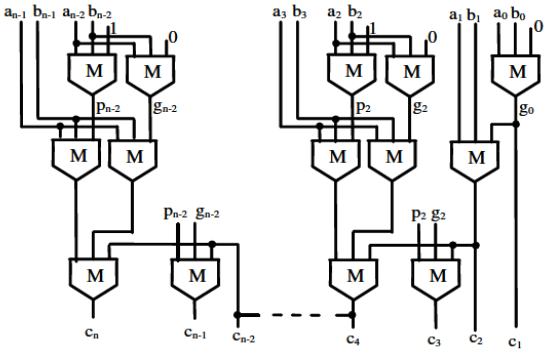
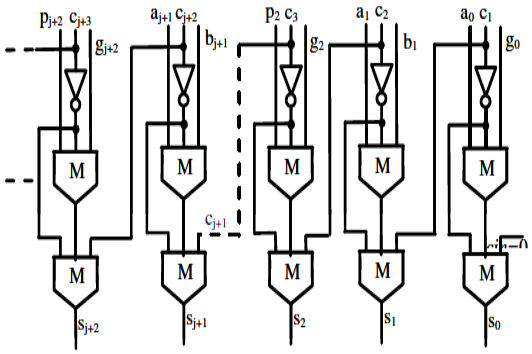


Fig: ARCHITECTURE OF BASIC NOVEL 2-BIT ADDER

To introduce the novel architecture proposed for implementing ripple adders in QCA, let consider two *n*-bit addends $A = an-1, \ldots, a0$ and $B = bn-1, \ldots, b0$ and suppose that for the *i* th bit position (with $i = n - 1, \ldots, 0$) the auxiliary propagate and generate signals, namely $pi = ai + bi$ and This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.$gi = ai \cdot bi$, are computed. *ci* being the carry produced at the generic $(i-1)$th bit position, the carry signal $ci+2$,furnished at the $(i+1)$the bit position.



(a)



(b)

(b)

Fig Novel *n*-bit adder (a) carry chain and (b) sum block.

IV. CONCLUSION

The reduced number of gates of this work offers the great advantage in the reduction of area and also the total delay. The QCA architecture is therefore, low area, low delay, simple and efficient for VLSI hardware implementation. It would be interesting to test the design of the modified 128-bit Novel adders.

V. ACKNOWLEDGMENT

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REFERENCES

[1] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernestein, "Quantum cellular automata," *Nanotechnology*, vol. 4, no. 1, pp. 49–57, 1993.

[2] M. T. Niemer and P. M. Kogge, "Problems in designing with QCAs Layout = Timing," *Int. J. Circuit Theory Appl.*, vol. 29, no. 1,pp. 49–62, 2001.

[3] J. Huang and F. Lombardi, *Design and Test of Digital Circuits by Quantum-Dot Cellular Automata*. Norwood, MA, USA: Artech House,2007.

[4] W. Liu, L. Lu, M. O'Neill, and E. E. Swartzlander, Jr., "Design rules for quantum-dot cellular automata," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2011, pp. 2361–2364.

[5] K. Kim, K. Wu, and R. Karri, "Toward designing robust QCA architectures in the presence of sneak noise paths," in *Proc. IEEE Design, Autom. Test Eur. Conf. Exhibit.*, Mar. 2005, pp. 1214–1219.

[6] K. Kong, Y. Shang, and R. Lu, "An optimized majority logic synthesis methology for quantum-dot cellular automata," *IEEE Trans. Nanotechnology*.vol. 9, no. 2, pp. 170–183, Mar. 2010.

[7] K. Walus, G. A. Jullien, and V. S. Dimitrov, "Computer arithmetic structures for quantum cellular automata," in *Proc. Asilomar Conf.Sygnals, Syst. Comput.*, Nov. 2003, pp. 1435–1439.

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