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Reusability of test bench of UVM for Bidirectional router and AXI bus

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ABSTRACT:
The predictive analysis of the design to ensure that, it will perform the given I/O function is performed through functional verification. Verification has become the dominant cost in any of the design process. The modernization of functional verification has become necessary task in verifying a large design. The project focuses on designing the Bidirectional network on chip router through virtual channel regulator and then AXI bus and thus developing the common verification environment for both the designs to show the reusability of test bench. The bidirectional network on chip router is implemented with unified buffer structure called the dynamic virtual channel regulator. The project also aims to develop a shortest path algorithm when a packet of data is to be transmitted as many paths are available thus by designing two routers. The functionality of the design is verified by using the latest Universal verification methodologies (UVM) further with the employment of reusable test benches of UVM for both the designs. The Verification goes on with which it finds functional coverage, state coverage, code coverage and toggle coverage of the Network on Chip Router by using Questa-Sim/cadence NC simulator and the synthesis is done by using Xilinx ISE 14.3i EDA Tools.

KEYWORDS: *Universal verification methodologies, virtual channel regulator, Open verification methodology, verification methodology module, AXI interconnect.*

I. INTRODUCTION

The process of demonstrating the functionality of the design has become one of the major tasks in today's era of multi-million gate ASICs and FPGAs. Verification consumes about 70% of the design effort. The number of verification engineer is more than the design engineers so the challenge of verifying a large design is growing exponentially. There is a need to define new methods that makes functional verification easy. Several strategies in the recent years have been proposed to achieve good functional verification with less effort. The recent advancement is to develop a methodology to reduce the time taken for verification. The advancement in the verification environment should be such that it reduces the re-spin of the ASIC design due to functional bugs and thus reducing the time to market.

This project helps one to understand about the latest verification methodologies, programming concepts like Object Oriented Programming of Hardware Verification Languages for the high quality verification with automation. This project is intended in building the reusability of test bench for the designed bidirectional network on chip router through virtual channel regulator and the AXI bus using the latest UVM verification methodologies.

II. MOTIVATION FOR THE WORK

The process of modernizing the verification methodology to reduce the time taken for verification can be accomplished by using the latest universal verification methodology (UVM). UVM is a combined effort of designers and tool vendors, based on the successful OVM and VMM methodologies. Its main promise is to improve test bench reuse, make verification code more portable and thus create a new market. The reusability of this verification environment is demonstrated by designing a bidirectional network on chip router through virtual channel regulator along with the shortest path algorithm for routing and also designing the AXI bus.

III. LITERATURE SURVEY

Chow.K.W.Y., (1994) mentioned in his paper that the early stages of design was verified by design engineer only using Verilog tasks and functions due to which all the test cases was not met and also time to market was not able to reach efficiently. Lot of time was spent in verification rather than design [1].

Few years later the System Verilog language was introduced by Accellera in 2002 and as IEEE Standard 1800-2005 in 2005. In 2009, the standard was merged with the base Verilog (IEEE 1364-2005) standard, creating IEEE Standard 1800-2009. The current version is IEEE standard 1800-2012. It is the first hardware verification language.

Moorby.P., (2004) in 17th International conference proposed the several aspects of this new language and how they form a critical part in the new design for verification paradigm [2].

McMahon, Anthony , O'Keeffe, Niall, Keane Kevin ,O'Reilly, James., (2008) presented a paper on System Verilog Verification Methodology Manual (VMM) was the first successful and widely implemented set of practices for creation of reusable verification environments in System Verilog, created by Synopsys, one of the strong proponents of System Verilog[3].

S. Iman., (2008) published a paper on "Step-by-step functional verification with System Verilog and OVM", with the new verification methodology named OVM. OVM is the library of objects and procedures for stimulus generation, data collection and control of verification process. It is available in System Verilog and System C [4].

Jae-Beom Kim, Nam-Do Kim, Byeong Min., (2011) published a paper on Universal verification methodologies (UVM), which is considered to be the common verification methodology [5].

T Lakshmi Priyanka, G. Deepthi, B. Sunil Kumar., (2013) Proposed the concept of reusability of test benches with the latest verification methodology i.e. UVM with the design of a router for network on chip communication in the paper "Reusable test bench for network on chip router using advanced verification methodologies. The paper explains about the perl script to provide automation in verification [6].

M. Bechtel Brabi and Dr. A. Rajalingam., (2012) illustrated in their paper "Recent survey for Bi-Directional network on chip pipelined architecture" that bidirectional network on chip router is more efficient than the conventional architecture. The paper also evidenced about the reduced latency & buffer size, increase in bandwidth and also indicated that pipelined architecture is more useful than the parallel architecture [7].

Ying-CherngLan, Hsiao-An Lin, Shih-HsinLo , Yu Hen Hu, Sao-Jie Chen.,(2011) published paper on " A Bidirectional NOC architecture with dynamic self-reconfigurable channel", in this paper they explained the concept of dynamic self-reconfigurable channel using an (CDC) channel direction control algorithm to avoid deadlock and starvation conditions. These results exhibit consistent and significant performance advantage over conventional NoC equipped with hard-wired unidirectional channels [8].

Mr. Ashish Khodwe , Prof. C.N. Bhoyar., (2013) published a paper on Bidirectional Network on chip Router through Virtual Channel Regulator, which dynamically allocates virtual channel and buffer resources according to network traffic conditions [9].

Baoxian Zhang, JieHao, and Hussein T. Mouftah., (2012) published a paper on "Bidirectional Multi-Constrained Routing Algorithms" in order to demonstrate an algorithm to find the shortest path of transfer of packets whenever many routing paths are available or when an congestion occurs [10].

Xu Chen, Zheng Xi, and Xin-An Wang., (2013) presented a paper on "Development of verification environment for AXI Bus using system Verilog". The paper explained about the methodology of verifying an AXI bus using system Verilog [11].

Pan Guoteng, Luo Li, OuGuodong, Fu Qingchao, Bai Han., (2013) proposed a paper on " Design and verification of a MAC controller based on AXI bus" this paper explained about the verification of AXI bus using an VMM [12]. The literature survey performed in this section specifies the researches carried out on the various verification methodologies and also on the design of the router which is considered to be the fundamental unit in an NOC. The related problem definition, objectives and methodology has been explained in next section.

3.1. Problem formulation

- During the recent years modernization of verification methodologies has become major criteria in order to reduce the time taken for verification and to reduce time to market. From the literature survey it is understood that even though the System Verilog is standard hardware description language.

There should be common verification methodologies because in reality most of the procedure in the test bench will be same for different project.

- The design of a generic or conventional router with statistically allocated buffer can cause the Head-of-Line blocking problem. In order to improve the performance and thus reducing the queue blocking, the dynamic buffer allocation significantly increases buffer usage.
- The methodology for developing the verification environment for AXI bus in proposed only by using system Verilog or by VMM, it is necessary to upgrade the verification of AXI bus using UVM.

3.2. Aim of the project

The aim of this paper is the design and implementation of Bidirectional network on chip router through virtual channel regulator with the shortest path algorithm and AXI bus. The designed system is verified using the latest verification methodologies i.e., the standard is Universal verification methodologies (UVM), which supports all of Verilog, system Verilog syntax along with automation techniques and thus observing the code coverage and functional coverage and thus signifying the reusability of the test bench for the bidirectional router and AXI bus.

IV. METHODOLOGY

The need for modernized common verification environment called UVM thus used the concept of reusability of test bench. In this paper to show the reusability of test bench two stages of design is being performed. First is designing the proposed bidirectional router with virtual channel regulator and the second is designing AXI interconnect. Both of these designs are verified under common verification environment called UVM thus showing the reusability of test bench.

V. DESIGN FLOW

The design flow of the project involves two stages, first is the design and implementation of Bidirectional network on chip router through virtual channel regulator and AXI bus demonstrated in block below. The second stage is developing a common verification environment called (UVM) and thus checking the reusability of test benches for both the designs.

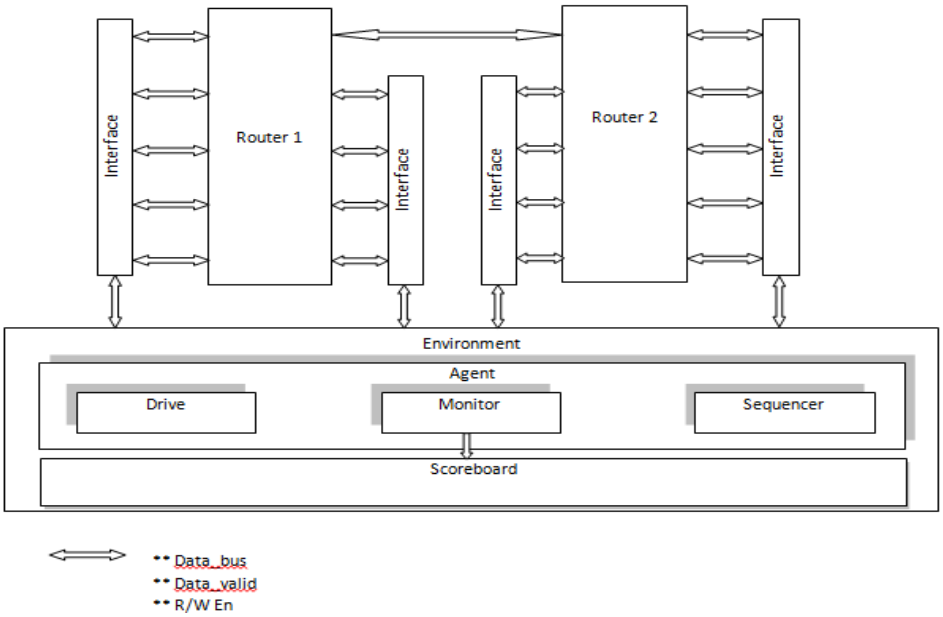

Figure 1. Flow diagram of Bidirectional routers with verification environment

The Figure.1 is the flow diagram of designing two bidirectional routers with the virtual channel regulator and the shortest path algorithm is implemented when many numbers of paths are available. The two interfaces are virtual interfaces and the packet transfer occurs through dynamic buffer allocation.

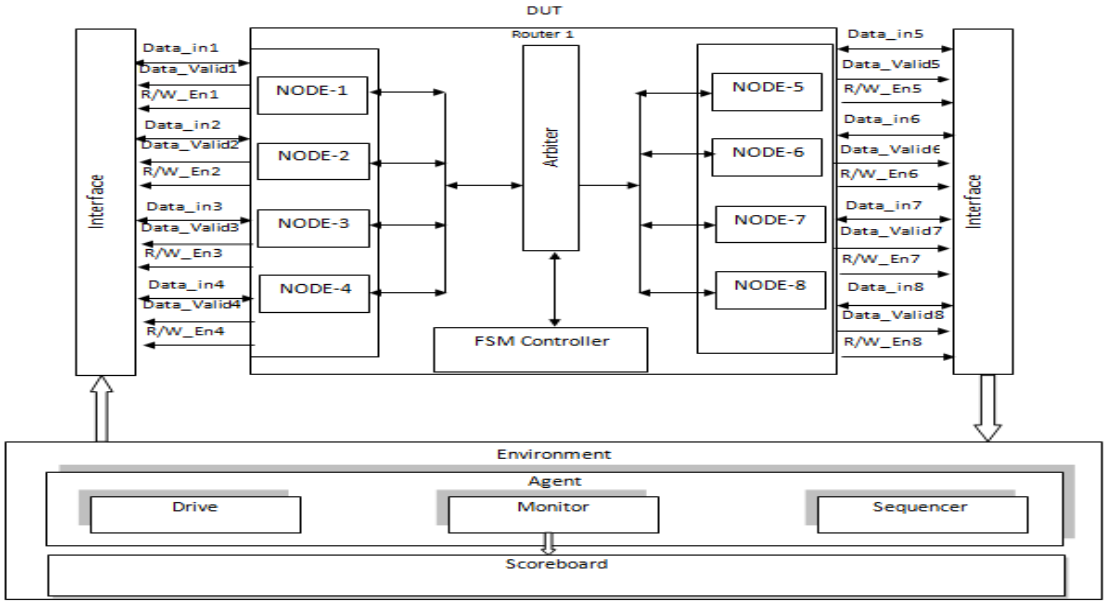

Figure 2. Flow diagram of design of each router

The Figure.2 is the flow diagram of design of each of the router. The router consists of register, FSM controller and the FIFOs where the input and output blocks are connected to the virtual interfaces. Arbiter is used in order to resolve the conflict when two or more packets of data makes a request to transmit a data in the same channel, in such case arbiter makes decision depending on the priority. The designed system is connected to the verification environment to check the functionality of the design.

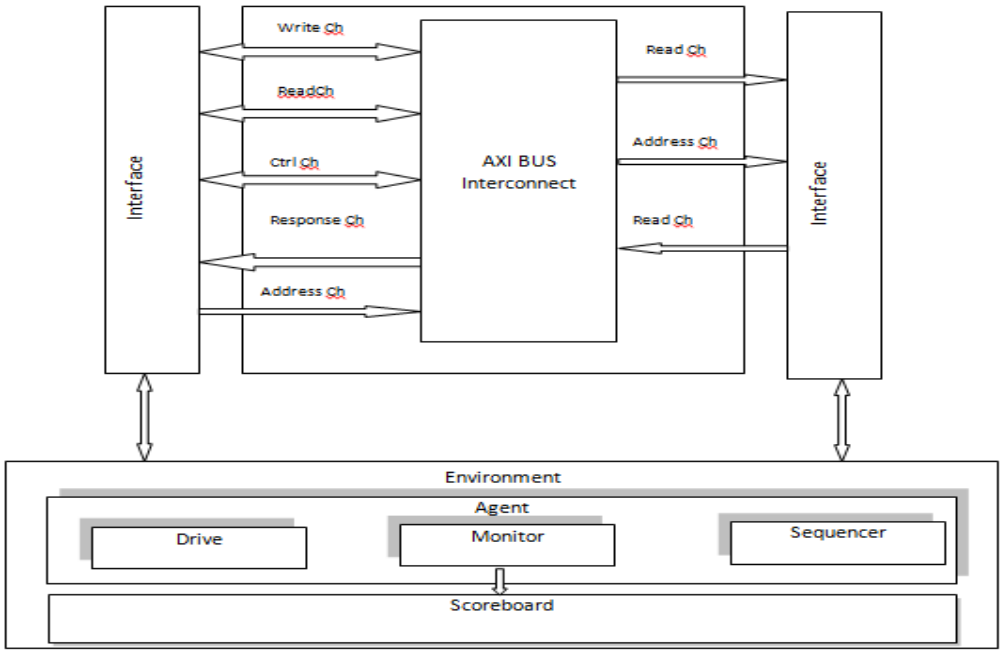

Figure 3. Flow diagram of designing AXI Bus interconnects.

The Figure.3 is the flow diagram of designing AXI Bus interconnects is the second part of the design. The AXI master and slave performs the read and write data depending on the request and grants. It is connected to the verification environment to check the intent of the design.

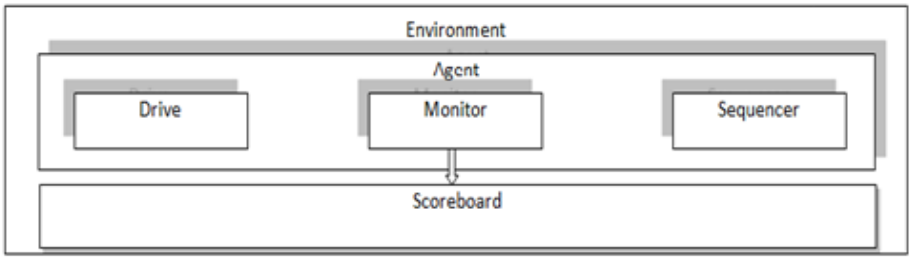

Figure 4. UVM Verification Environment

5. Results & Discussion

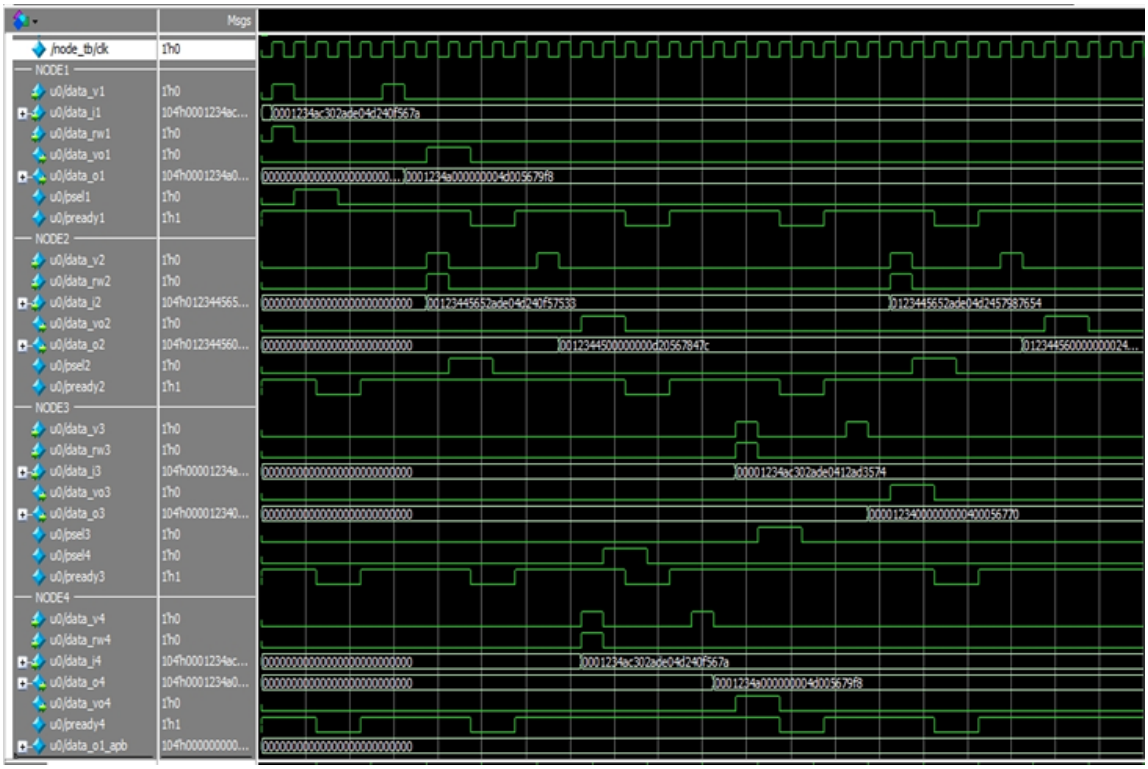

Figure.5. Simulated waveform of design of four nodes

The Figure.5 is the simulated waveform of design of the four node obtained in modelsim with the design of arbiter called round robin arbiter with APB bus. Further design is continued with the implementation of many such nodes for two routers and then designing & implementation of shortest path algorithm and then following the switch design.

VI. CONCLUSION AND FUTURE WORK

6.1. Conclusion

The result above is for generating a packet of data by creating four nodes and thus designing the round robin arbiter with APB bus. The UVM drives the input to these nodes for further verification process.

6.2. Future work

The above result is continued with the design and implementation of many such nodes with the shortest path algorithm to transmit the data packet to the other router.

The second stage is designing the AXI interconnect with the packet data transferred from AXI master and AXI slave by reading the data from the memory.

The third and the final stage is verification of these two designs by using the common verification environment with the reusable test bench and thus showing the reusability of test bench.

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