Design and Simulation of Nonisolated ZVZCS Resonant PWM Converter for High Step-Up and High Power Applications

S.M.MohamedSaleem, K.KalaiRaja¹, A.MohamedIlyasMydeen², C.R.Mohan Raj³, M.Hazina⁴

¹UG Scholars, **Asst. professor, Syed Ammal Engineering College, Ramanathapuram Tamil Nadu, India

I. INTRODUCTION

Recently, high step-up dc-dc converters do not require isolation have been used in many applications such as dc back-up energy systems for Uninterruptible Power Systems (UPS), renewable energy systems, fuel cell systems and hybrid electric vehicles. Generally, the high step-up dc-dc converter for these applications has the following requirements.

[1] High step-up voltage gain. Sometimes the voltage gain could be more than 10.

In order to provide high output voltage, the classical boost converter should operate at extremely duty cycle and then the rectifier diode must sustain a short pulse current with high amplitude. This results in severe reverse recovery as well as high EMI problems. Using an extremely duty cycle may also lead to poor dynamic responses to line to load variations. Moreover, in the high step up dc-dc converter the input current is usually large, and hence low voltage rated MOSFETs with small RDS(ON) are necessary in order to reduce the dominating conduction loss. However, the switch in the classical boost converter should sustain high output voltage as well, and therefore, the device selection is faced with a contradiction. A lot of step-up dc-dc converter topologies have been presented to overcome the aforementioned problem. Converters with Coupled inductors [1]-[5] can provide high output voltage without using high duty cycle and yet reduce the switch voltage stress. The reverse recovery problem associated with rectifier diode is also alleviated. However, they have large input current ripple and are not suitable for high power applications since the capacity of the magnetic core is considerable. The switched-capacitor converter [6]-[10] does not employ an inductor making it feasible to achieve high power density. However, the efficiency could be reduced to allow output voltage regulation. The major drawback of these topologies is that attainable voltage gains and power levels without degrading system performances are restricted. Most of the coupled-inductor and switched-capacitor converters are hard switched and therefore, they are not suitable for high efficiency and high power applications. Some soft switched interleaved high step-up converter topologies [11]-[18] have been proposed to achieve high efficiency at desired level of voltage and power level.

In this paper, a new interleaved soft switched high step-up dc-dc converter for high efficiency, high voltage applications are presented. The proposed converter has the following advantages.

[1] Reduced voltage stresses of switches and diodes.
[2] ZVS turn-on the switches and ZCS turn-off the diodes.
[3] Low input current ripple due to interleaved structure.
[4] Reduced energy volumes of most passive components.
[5] Extendibility to desired voltage gain and power level.

ABSTRACT

This paper proposes a generalized scheme of new soft-switched interleaved boost converters that is suitable for high step-up and high power applications. The proposed converter is configured with proper numbers of series and parallel connected basic cells in order to fulfill the required output voltage and power levels respectively. This leads to flexibility in device selection resulting in high component availability and easy thermal distribution. Design examples of determining the optimum circuit configuration for given output voltage gain of 8.75 times is presented.

KEY WORDS: High Step-Up, High Voltage Gain, Multiphase, Non-isolated, Soft Switched.
The operating principles along with a design example of the proposed converter are described. Experimental results from a 1.5-kW prototype are also provided to validate the proposed concept.

II. PROPOSED INTERLEAVED HIGH STEP-UP CONVERTER

2.1. General Architecture

Fig. 1 shows the Architecture of the proposed converter. The single phase AC supply is converted into DC supply and applied to boost converter. Due to two limb topology the output power is greatly increased compared to that of conventional converter. The switch is controlled by means of PWM technique. Hence controlled DC voltage is applied to the DC Load.

B. GENERALIZED MULTIPHASE DC-DC CONVERTER

Fig. 2 shows a basic cell used as a building block to build the proposed high step-up converter. The basic cell consists of an input filter inductor, a switch leg and diode leg, and an auxiliary inductor, and capacitor.

Fig. 3 shows the generalized circuit of the proposed converter with $N$ and $P$, where $N$ is the number of output series-connected basic cell and $P$ is the number of output parallel-connected basic cell, respectively, meaning that there exist totally $NP$ basic cells. The diode leg of $n$th basic cell is connected to the output capacitor $C_{3,n}$, where $n=1, 2, 3, \ldots, N$ and $p=1, 2, 3, \ldots, P$, and output capacitors $C_{3,1}$ to $C_{3,N}$ are connected in series on top of output capacitor $C_1$ to form the output voltage. That is, “$N$” could be increased to get higher output power. It should be noted that the voltage rating of switches can be reduced by reducing $N$ and the current rating of them can be reduced by increasing $N$ or $P$. Also, the voltage and current ratings of diodes can be reduced by increasing $N$ and $P$, respectively. Therefore, optimum devices in the sense of cost and availability can be selected proper choice of $N$&$P$. The interleaving technique can be applied to reduce the size of input filter inductors and output filter capacitors. Therefore, “$N$” and “$P$” can properly be chosen according to given output voltage and power level. This could give flexibility in device selection resulting in optimized design even under harsh design specifications.
III. CIRCUIT DIAGRAM

Fig. 4. shows the circuit diagram of the proposed converter which has the same circuit topology as the PWM method proposed in [14]. Fig. 5. shows key waveforms illustrating the operating principle of the proposed converter. The proposed converter consists of a general boost converter as the main circuit and an auxiliary circuit which includes capacitor $C_r$, inductor $L_r$ and two diodes $D_L$ and $D_U$.

Two switches are operated with asymmetrical complementary switching to regulate the output voltage. Owing to the auxiliary circuit, not only output voltage is raised but ZVS turn-on of two switches can naturally be achieved in CCM by using energy stored in filter inductor $L_f$ and auxiliary inductor $L_r$. Unlike PWM method [14] in which the switches are turned OFF with high peak current the proposed converter utilizes $L_r$-$C_r$ resonance of auxiliary circuit, thereby reducing the turn-off current of switches. Furthermore, for resonance operation, the capacitance of $C_r$ is reduced volume. Also, switching losses associated with diode reverse recovery of the proposed RPWM converter are significantly reduced.

IV. OPERATING PRINCIPLE

The operating modes and key waveforms of the proposed converter are shown in Figs. 5 and 6. In the below resonance operation, five modes exist within $T_s$. Mode 1 ($t_0 - t_1$): This mode begins when upper switch $S_U$ which was carrying the current of difference between $i_{Lf}$ and $i_{Lr}$ is turned OFF. $S_L$ can be turned ON with ZVS if gate signal for $S_L$ is applied before the current direction of $S_L$ is reversed. Filter inductor current $i_{Lf}$ and auxiliary current $i_{Lr}$ starts to linearly increase and decrease, respectively, as follows

$$i_{Lf}(t) = \frac{V_i}{L_f}(t - t_0) + i_{Lf}(t_0)$$

$$i_{Lr}(t) = \frac{V_{C_r,min} - V_o}{L_r}(t - t_0) + i_{Lr}(t_0)$$

This mode ends when decreasing current $i_{Lr}$ changes its direction of flow. Then $D_U$ is turned OFF under ZCS condition.

Mode 2 ($t_1 - t_2$): This mode begins with $L_r$-$C_r$ resonance of the auxiliary circuit. Current $i_{Lf}$ is still linearly increasing. The voltage and current of resonant components are determined, respectively, as follows:
\[ i_{Lr}(t) = -i_{Cr}(t) = \frac{V_{r,2}}{Z} \sin(\omega_r(t - t_1)) \]

\[ v_{Cr}(t) = V_{r,2} \left[ \cos(\omega_r(t - t_1)) - 1 \right] + v_{Cr}(t_1) \]

Fig. 5. Key waveforms of the proposed converter

Where \( V_{r,2} = V_{r,\text{min}} - V_{r,\text{max}} \), \( Z = \sqrt{L_r/C_r} \) and \( \omega_r = 1/\sqrt{L_r/C_r} \). This resonance mode ends when \( i_{Lr} \) reaches to zero. Note that \( D_L \) is turned OFF under ZCS condition.

Mode 3 \((t_2 - t_3)\): There is no current path through the auxiliary circuit during this mode. Output capacitors supply the load. At the end of this mode the turn-off signal of \( S_L \) is applied. It is noted that the turn-off current of \( S_L, I_{SL,\text{off}} \) is limited to filter inductor current at \( t_3, I_{L,\text{max}} \), which is much smaller than that of PWM method.

Mode 4 \((t_3 - t_4)\): This mode begins when lower switch \( S_L \) is turned OFF. \( S_U \) can be turned ON with ZVS if gate signal for \( S_U \) is applied before the current direction of \( S_U \) is reversed. Filter inductor current \( i_{L_f} \) starts to linearly decrease since voltage \( V_{L_f} \) becomes negative

\[ i_{L_f}(t) = \frac{V_i - V_{C1}}{L_f} (t - t_3) + i_{L_f}(t_3). \]

Like Mode 2, the other \( L_r-C_r \) resonance of auxiliary circuit is started, and \( D_U \) starts conducting. The voltage and current of resonant components are determined, respectively, as follows:
\[ i_{t} = -i_{c}(t) = \frac{V_{r}}{Z} \sin(\omega_{r}(t - t_{3})) \]

\[ V_{c}(t) = V_{r} \left[ \cos(\omega_{r}(t - t_{3})) - 1 \right] + v_{c}(t_{3}) \]

where \( V_{r} = V_{C_{1}} + V_{C_{2}}, \) \( Z = \sqrt{L_{r}/C_{r}}, \) and \( \omega_{r} = 1/\sqrt{L_{r}/C_{r}}. \)

This mode ends when \( i_{l_{r}} \) is equal to \( i_{l_{y}}. \)

**Mode 5 (t_{4} – t_{5}):** After \( i_{l_{r}} \) equals \( i_{l_{y}}, \) \( i_{l_{y}} \) changes its direction, then this mode begins. At the end of this mode, turn-off signal of \( S_{y} \) is applied and this mode ends.

**V. VOLTAGE CONVERSION RATIO**

To obtain the voltage gain of the proposed converter, it is assumed that the voltage across \( C_{1} \) and \( C_{2} \) are constant during the switching period \( T_{s}. \) The output voltage is given by

\[ V_{o} = V_{C_{1}} + V_{C_{2}} \]

It can also be expressed as

\[ V_{o} = \frac{2}{1 - D_{eff}} V_{i} = \frac{2}{1 - D} V_{i} - \Delta V \]

where effective duty \( D_{eff} \) and voltage drop \( \Delta V \) are expressed using duty loss \( \Delta D. \)

\[ D_{eff} = D - \Delta D \]

\[ \Delta V = \frac{2\Delta D V_{i}}{(1 - D)(1 - D_{eff})}. \]

\[ V_{C_{1}} = \frac{1}{1 - D} \cdot V_{i}. \]

can be expressed as

Design is carried out for finding \( L_{r}, f_{r}, L_{y} \) and \( C_{r}. \)

**A. Design of \( L_{r} \)**

\( V_{C_{2}} \) can be expressed as

\[ V_{C_{2}} = \frac{1}{1 - D} V_{i} - \Delta V. \]

In the steady state, the average load current equals the average current of diodes \( D_{L} \) and \( D_{U}. \) Since \( i_{l_{r}} \) flows through the \( D_{L} \) during mode 2, the average load current can be obtained as follows.

\[ I_{DL,av} = \frac{V_{o}}{R_{o}} = \frac{2}{T_{s}} \int_{0}^{T_{s}/4} (V_{C_{r, min}} - V_{C_{l}}) \frac{\sqrt{C_{r}}}{\sqrt{L_{r}}} \sin(\omega_{r} t) \cdot dt \]

From the above equation, \( V_{C_{r, min}} \) and \( V_{C_{r, max}} \) can be obtained by,

\[ V_{C_{r, min}} \approx V_{C_{1}} - \frac{V_{o}}{2C_{r}R_{o}f_{s}} \]

\[ V_{C_{r, max}} \approx V_{C_{1}} + \frac{V_{o}}{2C_{r}R_{o}f_{s}}. \]

**VI. DESIGN OF THE PROPOSED CONVERTER**

The generalized scheme of the proposed converter has been shown in Fig.3., where it is configured with proper numbers of series and parallel connected basic cells. This leads to flexibility in device selection resulting
in high-component availability and easy thermal distribution. A specification for a design example in this paper is given as follows and the chosen circuit topology for the specifications is shown in Fig.4.

\[ P_0 = 220\ W,\ V_0 = 105\ V,\ V_i = 12\ V,\ f_s = 15\ kHz,\ \Delta I_{in} = 20\%,\ \Delta V_{o} = 3\% \]

Considering input current ripple \( \Delta I_{in} \) input inductor \( L_f \) is determined by,

\[ L_f = 0.5(1-D)\frac{V_{in}}{\Delta I_{in}} f_s = 70\mu H. \]

B. Design of \( f_r \)

Due to the smaller switch turn off current and duty loss, the below-resonance operation is chosen, and the resonant frequency \( f_r \) can be obtained from

\[ f_r = \frac{1}{2\pi\sqrt{L_rC_r}} \] and

\[ f_r = \frac{1}{2D_{eff}} \]

So. \( f_r \leq 42\ kHz \)

C. Design of \( L_r \) and \( C_r \)

From the resonant frequency \( f_r \),

\[ L_r = 3\ \mu H \& \]

\[ C_r = 4.7\ \mu F \]

The improvement of the proposed RPWM method compared to PWM method are summarized as follows.

1) Due to the reduced operation duty, the rms current ratings of the switches are reduced by 5-15%, resulting in reduced conduction losses.

2)Due to the resonant operation, the turn-off current of switches are reduced by 25-60% and falling slopes of the diode current are reduced, resulting in significantly reduced switching losses.

3)The required capacitance of auxiliary capacitor is dramatically reduced to 1/20th resulting in reduced volume and cost.

### VII. SIMULATION CIRCUIT

Fig(a) Input voltage
V. CONCLUSION

In this paper, an RPWM method switching method has been proposed for high step-up soft switching dc-dc converter. The proposed converter has the following advantages:

a. ZVS turn-on of the active switches in CCM.
b. Negligible diode reverses recovery due to ZCS turn-off of the diodes.
c. Greatly reduced passive components and voltage ratings.
d. Its voltage gain is 8.75 times, is doubled with the classical boost converter.
REFERENCES


ACKNOWLEDGEMENT

Mohamed Saleem. S.M. is currently pursuing the B.E Degree in Electrical and Electronics Engineering from Syed Ammal Engineering College, Anna University, Chennai, India. His current research interests include design and implementation of new interleaved soft switching boost converter with high step-up applications.

KalaiRaja.K are currently pursuing the B.E Degree in Electrical and Electronics Engineering from Syed Ammal Engineering College, Anna University, Chennai, India. His current research interests include design and implementation of new interleaved soft switching boost converter with high step-up applications.

Mohamed Ilyas Mydeen.A are currently pursuing the B.E Degree in Electrical and Electronics Engineering from Syed Ammal Engineering College, Anna University, Chennai, India. His current research interests include design and implementation of new interleaved soft switching boost converter with high step-up applications.

MohanRaj.C.R. are currently pursuing the B.E Degree in Electrical and Electronics Engineering from Syed Ammal Engineering College, Anna University, Chennai, India. His current research interests include design and implementation of new interleaved soft switching boost converter with high step-up applications.

Hazina.M received the B.E degree from Anna University Chennai in 2010 and M.E degree from the same university in 2012. She is currently working as an assistant professor in Syed Ammal Engineering College, Ramanathapuram, Tamilnadu, India. Her current research interests include design and implementation of new interleaved soft switching boost converter with high step-up applications.