Comparative study of capacitance of Nano-Scale and Pico-scale-MOSFET

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ABSTRACT
As CMOS technology dimensions are being aggressively scaled to reach a limit where device performance must be assessed against fundamental limits, pico scale device modeling is needed to provide innovative new MOS devices as well as to understand the limits of the scaling process. This paper presents a comparison between nanoscale and pico scale MOSFETs from the viewpoint of device physics. The MOS capacitance for different dielectric is compared for device dimensions in nanometer and pico meter using MATLAB.

Keywords: Channel length, Gate oxide thickness, Gate capacitance, dielectric constant, nanometer, Pico meter, Threshold voltage.

I. INTRODUCTION
The metal–oxide–semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET) is a transistor used for amplifying or switching electronic signals. The MOSFET behaves as a capacitor as there is a dielectric layer in between semiconductor and metal.

![MOSFET Diagram](image)

The gate of the Mos is a good capacitor. Its capacitance attracts the Charges to invert the channel. So, Higher the capacitance higher will be drain current.

Capacitance Comparison

We have
\[ C_g = C_{ox}WL \]

\( C_g \) = Gate capacitance, \( W \) = width of dielectric,
\( C_{ox} \) = oxide capacitance, \( L \) = Length of dielectric

We have,
\[ C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \]

\( \varepsilon_{ox} = K \varepsilon_0 \)
\( \varepsilon_0 \) = permittivity in free space
\( k \) = Dielectric constant
Comparative study of capacitance of Nano-Scale and Pico-scale-MOSFET

We have $k (SiO_2) = 3.9$

And the value of thickness and width of the have taken up to 5 nanometer.

Let us change the value of dielectric constant ($K$):

1) If $k < 3.9$, Threshold voltage Increases.

2) If $k > 3.9$, Threshold voltage Decreases.

So changing the value of $k$ where $k > 3.9$

And take the value of W, L in bellow 5 nanometer.

If we plot $Cox$ Vs $Tox$

1) Taking the value of $Tox$ in Nanometer
Comparative study of capacitance of Nano-Scale and Pico-scale-MOSFET

k=3.9 to 6.4
k=6.9 to 9.4

k=9.9 to 11.9
k=11.9 to 14.4

2) Taking the Tox in Picometer
Comparative study of capacitance of Nano-Scale and Pico-scale-MOSFET

K=3.9 to 6.9
K=7.4 to 11.9

To study Cg vs. Cox
We have

\[ C_g = Cox \cdot W \cdot L \]

From above plotted graphs, using \[ Cox = 0.08:0.01:0.20; \]

Case 1: taking W in nanometer

W=2 to 5nm
CONCLUSION

There are a number of issues in scaling MOSFET devices, particularly for the sub-100 nm technology evolution. The most critical issue is the gate dielectric, because very thin gate oxides are required for sub-100 nm generations. For such thin oxides, gate leakage current due to direct tunneling becomes unacceptably large. In order to decrease the leakage current due to tunneling, the physical thickness of the dielectric must increase, while the equivalent oxide thickness must continue to be reduced. Use of alternate gate materials with dielectric constant higher than that of silicon dioxide is the leading projected solution to reduce the gate leakage current to more tolerable levels. Therefore, modeling of the thin oxide related issues, such as gate direct tunneling current, gate capacitance, and capacitance reconstruction are crucial for further gate oxide scaling.

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REFERENCES