An Ultra-Low Power Physical Layer Design For Wireless Body Area Network

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Objective

WBAN for health monitoring consists of multiple sensor nodes. Each node is typically capable of sensing one or more physiological signals, processing these signals storing the processed data, transmitting the data to other nodes and/or a WBAN server. The main objective is to design physical layer with lower power consumption.

Index Terms: Digital circuit design, low power, wireless body area network (WBAN), wireless communication.

Abstract

The wireless body area network (WBAN) is a wireless network used for communication among sensor nodes operating on, in or around the human body in order to monitor vital body parameters and movements. The pursuit of higher quality of life motivates people to be more concerned about their health and potential diseases. At the same time, many patients can benefit from continuous monitoring of their diagnostic procedures. All these require a convenient healthcare surveillance system to monitor people's health status anytime and anywhere. The tracking capability of such a system should also be able to provide optimal maintenance after a surgical procedure and support early detection of abnormal health conditions.This paper investigates the efficient design of the PHY layer architecture for wireless body area networks (WBAN), which targets on ultra-low power consumption with reliable quality of service (QoS). A low cost baseband transceiver specification and a data processing flow are proposed with a comparatively low-complexity control state machine. A multifunctional digital timing synchronization scheme is also proposed, which can achieve packet synchronization and data recovery. To demonstrate and to optimize the reliability of the proposed design, the dedicated bit-error-rate and power analysis is reported. VHDL code is created to describe the PHY system and SPI and is verified on a Xilinx field-programmable gate array (FPGA) platform.

1. Introduction

The pursuit of higher quality of life motivates people to be more concerned about their health and potential diseases. At the same time, many patients can benefit from Continuous monitoring of their diagnostic procedures. All these require a convenient healthcare surveillance system to monitor people's health status anytime anywhere, especially when people suffer an acute event, such as a sudden heart attack. The tracking capability of such a system should also be able to provide optimal maintenance after a surgical procedure and support early detection of abnormal health conditions.Recent advances in sensors, integrated circuits, and wireless communication are paving the way for developing miniature, lightweight, ultra-low power physiological healthcare surveillance and monitoring devices for the improvement of human lives. These devices can be integrated into wireless body area networks (WBANs) for health monitoring. A WBAN topology consists of a series of miniature invasive/non-invasive physiological sensors and is able to communicate with other sensor nodes or with a central node. The central node has higher computational capability and communicates wirelessly with a personal server and subsequently the outside world through a standard telecommunication infrastructure, such as wireless local area networks and cellular phone networks. Potential applications of WBANs include chronic disease management, medical diagnostics, home-monitoring, biometrics, and sports and fitness tracking, etc.. The power budget is quite strict for WBAN applications because the wireless device is powered by a battery. An optimized low power low data rate digital baseband IC is proposed, and its performance is analyzed in detail. The proposed baseband transceiver is configured with a frequency-shift keying (FSK) modulation/demodulation module. A specified physical layer (PHY) architecture is developed, which reduces the complexity of baseband processing but maintains satisfactory performance. To recover precisely the timing and data information from an FSK demodulator, a novel synchronization and data recovery (SDR) scheme is proposed that has comparatively low complexity. To overcome the timing drift between the transmitter and receiver, a low-complexity sampling point realignment scheme is proposed. This scheme shares the same hardware with the SDR scheme and can automatically adjust to the correct sampling point during data transmission.

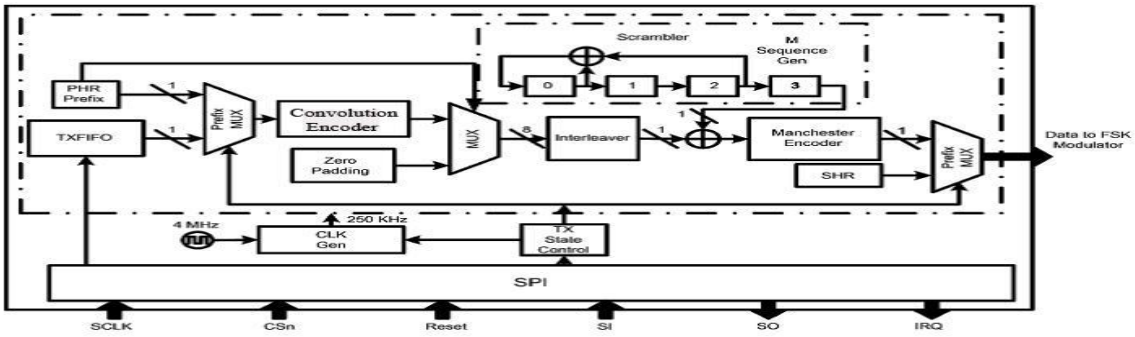
2. Existing Physical Layer Design:

The CC2420 from Texas Instruments in can cover a 20–30 m range at a power consumption of 60-70 μW and hamming encoding technique was used. However, such operation range and power consumption are not the optimal choice for WBAN applications. The transceivers which have high data rate transmission, resulting in comparatively high power consumption.

3. Modified Technique:

Baseband Transmitter

In the transmitter block, the Physical Layer Service Data Unit (PSDU) from the MAC layer is processed in the proposed transmitter (TX) baseband processor module to generate a physical layer protocol data unit (PPDU) packet. The channel coding and signal processing are performed on the PPDU in the TX baseband processor module and the raw data rate of the TX baseband processor module output is 250 kb/s. The baseband raw data is modulated by FSK and then directly up-converted to a 2.45 GHz RF signal. In the receiver (RX) block, the received RF signal is down-converted to a 2 MHz intermediate frequency (IF) signal and then demodulated by a low power FSK demodulator. The demodulated signal is processed by the proposed RX baseband processor module. Following that, the received PSDU is fed into the MAC layer. To achieve ultra-low power consumption, a low-complexity PHY specification is proposed. The signal processing flow for TX and RX are presented. In the TX module, the baseband processor receives the PSDU from the MAC layer and constructs the PPDU. The permitted length of the PSDU within one packet should be no larger than 127 octets and this information is contained in the PHY header (PHR) in octets. Once one packet of the PSDU is generated by the MAC layer, it is fed into TXFIFO and ready for transmission. There is a Prefix MUX block controlled by the TX state control block to select the input of the encoder block. The diagram of the transmitter block of the baseband transceiver is illustrated in the following figure.



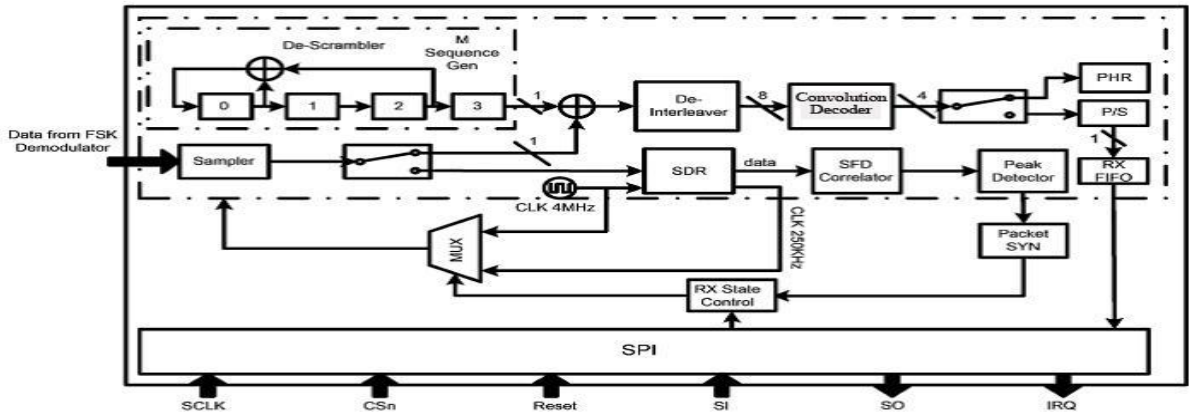
Transmitter Block

When a transmission command is sent from the MAC layer, the PHR is prefixed to the PSDU and sent into the Hamming encoder block first. The input data of the encoder block is in serial sequence with 1 bit word-length. In our design, convolution coding and interleaving techniques are used as forward error correction (FEC). For each consecutive bits of input data, the encoder block generates output data simultaneously . The output data of the convolution encoder block is fed into the matrix interleaving block to suppress the burst error. To eliminate long strings of like bits that might impair receiver synchronization and to eliminate most periodic bit patterns that could produce undesirable frequency components (including the dc component), the interleaved data payload is first fed into a scrambling block and then coded by a Manchester encoder.The scrambling block generates the scrambling code in serial sequence with 1 bit word-length. Here we use the sequence generator with as the scrambler to achieve satisfactory performance and comparatively low complexity. The output data of the interleaving block is in serial sequence with 1 bit word-length and is XOR with the generated scrambling code. The scrambled data payload is fed into the Manchester encoder. The Manchester encoder converts the bit "0" to bits "01" and converts the bit "1" to bits "10," and thus the total number of "0" and "1" can be balanced. The output of the Manchester encoder is prefixed with the synchronization header (SHR) and is sent to the FSK modulator for transmission.

4. Baseband Receiver

In the receiver module, the received data stream is the demodulated binary signals from the FSK demodulator. A D flip-flop is used provided by the technology library to sample and to restore the analog input. If the voltage of the input signal is higher than of the D flip-flop, the output of the D flip-flop will be "1." If the voltage of the input signal is lower than of the D flip-flop, the output of the D flip-flop will be "0." As illustrated in Figure, the signals are first

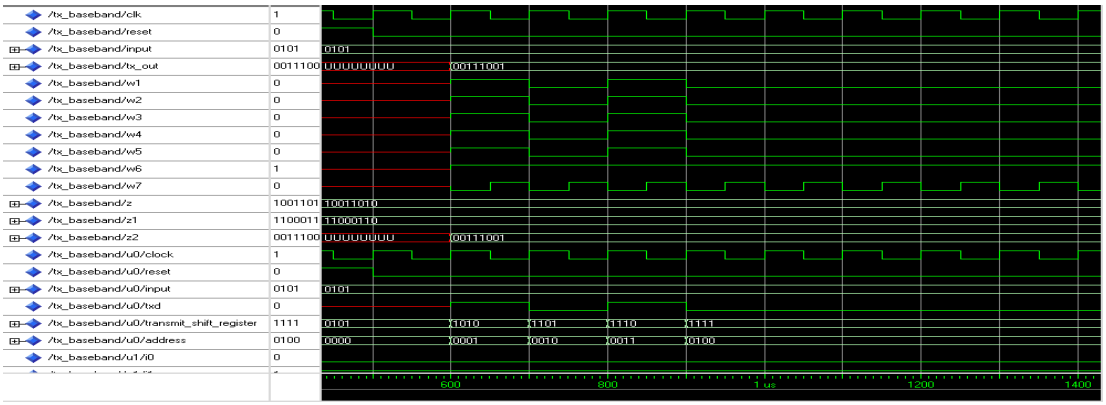
serially fed into the synchronization and data recovery (SDR) block to achieve synchronization and to recover the received data. The SDR block over-samples the incoming signal using a shift register matrix block and calculates the correlation between the incoming data and the predefined preamble sequence to achieve bit synchronization. The peak of the calculated correlation is continuously detected. Once the peak value is found, the start-of-frame delimiter (SFD) Correlate block calculates the correlations between the incoming data and the predefined SFD sequence, and the peak value is searched by the following peak detector block. Once the peak value is found, the packet synchronization is confirmed. The preamble sequence and SFD are removed and the Packet SYN block indicates to the RX State Control block that the PHR and PSDU can be received. The SDR block also generates the 250 kHz clock, and the RX State Control block selects the operation clock frequency of the RX baseband processor module which can be between 4 MHz clock and 250 kHz clock. Manchester decoding is first performed on the received PHR and PSDU data stream by detecting the first bit for every two continuous received bits. Following that, the incoming data is descrambled and the structure of the descrambling block is identical to that of the scrambling block. The output of the descrambling block has a 1-bit word-length, and XOR operations are completed with the incoming data bit by bit. Following that, the PHR and PSDU are fed into the FEC decoding block, which includes the de-interleaving block and convolution decoder block. The output of the de-interleaving block has an 1-bit word-length and is fed into the convolution decoder block.
The decoder block checks whether there is any error in the incoming data and corrects the error. If the decoder block detects an error but can not correct it, the receiver will stop receiving any data and the MAC layer will request a retransmission of this packet. The PHR is decoded first and thus length information about the PSDU can be obtained by the RX state control block. The word-length of the convolution decoder block output is 2 bits, and there is a parallel to serial buffer, so that bits in the PSDU are fed into the RXFIFO in serial sequence with 1 bit word-length, and is read by the MAC layer.



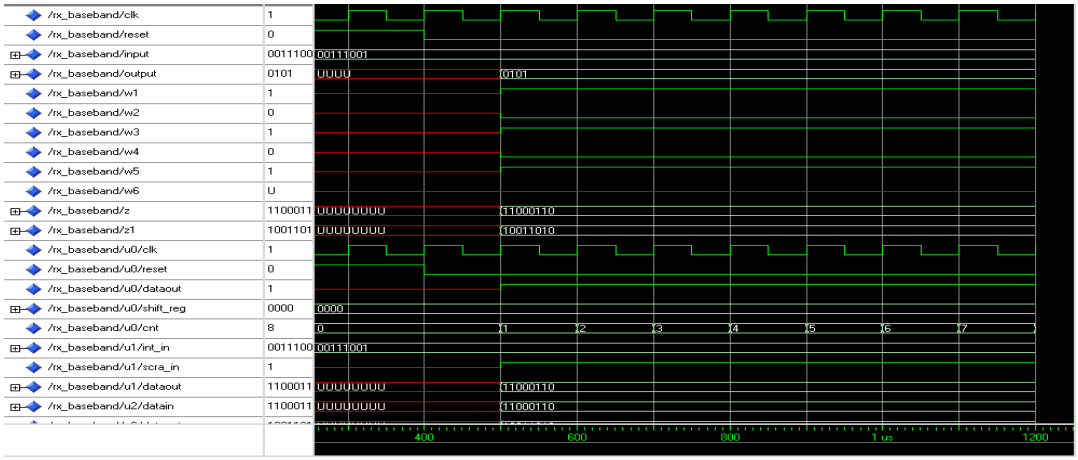
Receiver Block

5. Simulation Results:

Simulation Result Of Transmitter Baseband



Simulation Result Of Receiver Baseband

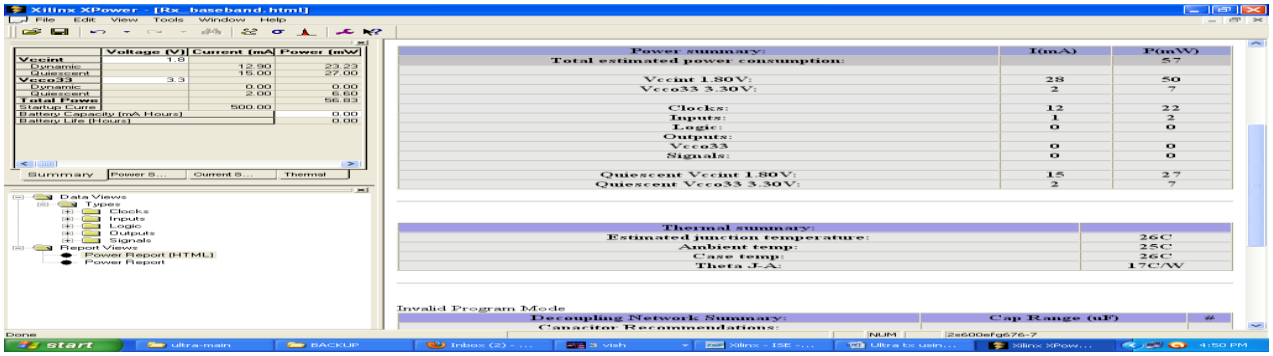


6. Existing Technique:

Power Estimation Of Existing Transmitter Block

Design:	C:\Xilinx\hamming\Tx_baseband.ncd	
Preferences:	Tx_baseband.pcf	
Part:	2s50eft256-7	
Data version:	PRELIMINARY,v1.0,07-31-02	
Power summary:	I(mA)	P(mW)
Total estimated power consumption:		76
Vccint 1.80V:	38	69
Vcco33 3.30V:	2	7
Clocks:	25	45
Inputs:	2	4
Logic:	1	2
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	10	18
Quiescent Vcco33 3.30V:	2	7

Power Estimation Of Existing Receiver Block



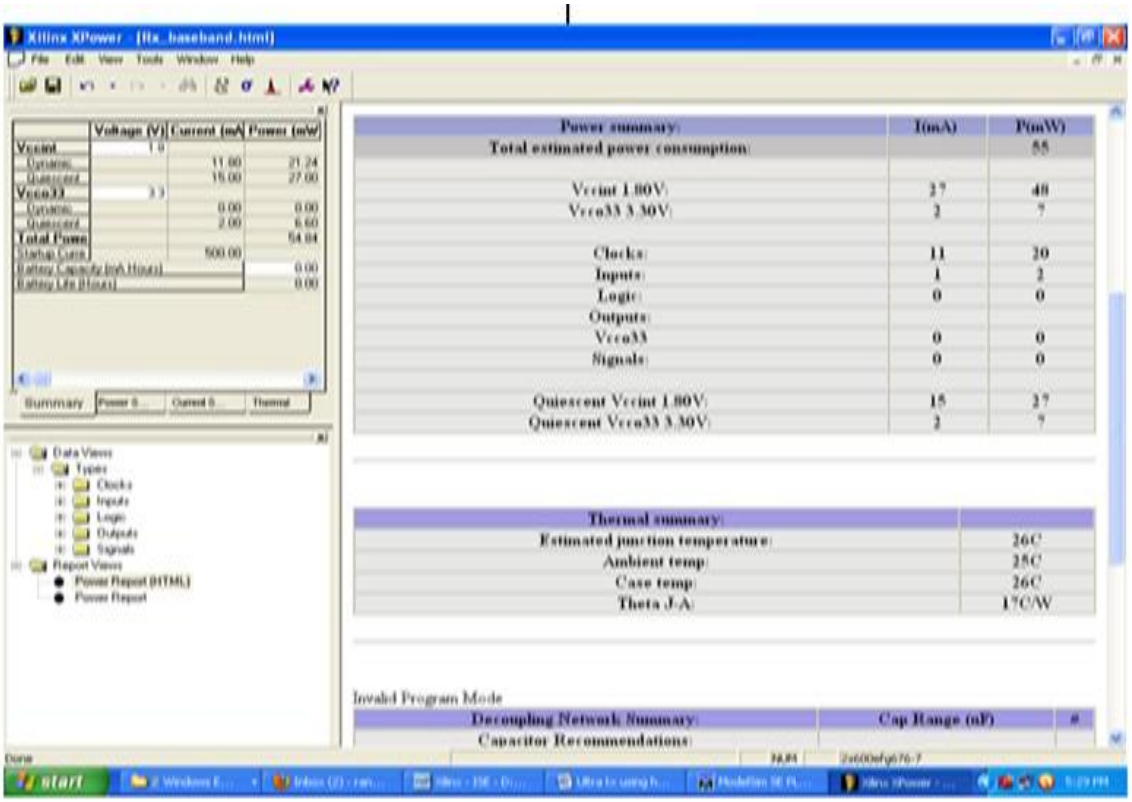
7. Modified Technique:

POWER ESTIMATION OF PROPOSED TRANSMITTER BLOCK

Design:	**C:\Xilinx\convolution\Tx_baseband.ncd**
Preferences:	**Tx_baseband.pcf**
Part:	**2s50eft256-7**
Data version:	**PRELIMINARY,v1.0,07-31-02**

power summary:	I(mA)	P(mW)
Total estimated power consumption:		62
Vccint 1.80V:	31	55
Vcco33 3.30V:	2	7
Clocks:	17	31
Inputs:	2	4
Logic:	1	2
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	10	18
Quiescent Vcco33 3.30V:	2	7

POWER ESTIMATION OF PROPOSED RECEIVER BLOCK



POWER ANALYSIS TABLE:

Technique	Transmitter power	Receiver power
Hamming encoder (existing)	**55 mW**	**57mW**
Convolution encoder (proposed)	**50mW**	**55mW**

8. Conclusion

The efficient design of the PHY layer architecture for wireless body area networks (WBAN), which targets on ultra-low power consumption with reliable quality of service (QoS). A low cost baseband transceiver specification and a data processing flow are proposed with a comparatively low-complexity control state machine. A low power low data rate digital baseband transceiver IC is proposed, which uses low-complexity architecture to achieve satisfactory performance. The target power consumption is less. Benefiting from the novel low complexity hardware architecture design and optimized hardware implementation. Specified physical layer (PHY) architecture is developed, which reduces the complexity of baseband processing but maintains satisfactory performance. To recover precisely the timing and data information from an FSK demodulator, a novel synchronization and data recovery (SDR) scheme is proposed that has comparatively low complexity. A convolution code is a linear error-correcting code which can detect errors, and correct them; thus, reliable communication is possible between the transmitted and received bit patterns . To optimize the reliability of the proposed design, the dedicated bit-error-rate and power analysis is reported. VHDL RTL code is created to describe the PHY system and SPI and is verified on a Xilinx field-programmable gate array (FPGA) test platform.

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