Low Power Glitch Free Modeling in Vlsi Circuitry Using Feedback Resistive Path Logic

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Abstract
Low power has emerged as a principal theme in today's electronics industry. This work focus on the development of low power VLSI design methodology on system level modeling and circuit level modeling for power optimization. This work develops a power optimization approach in bus transitions using hamming coding scheme called 'Unbounded Lagger algorithm' for transition power reduction in VLSI design. The developed transition optimization approach further merged with circuit level power optimization using Glitch minimization technique. A resistive feed back method is developed for the elimination of glitches in the CMOS circuitry which result in power consumption and reducing performance of VLSI design. The proposed system is developed on Active HDL for designing a Bus transition Optimization algorithm using Unbounded Lagger algorithm, where an encoder and decoder units are designed for the minimization of transition for parallel bus transition in data transfer**.**

Introduction
In past, the major concerns of the VLSI designer were area, performance, cost and reliability; power consideration was mostly of only secondary importance. With advanced Nickel-Metal-Hydride (secondary) battery technologies offering around 65 watt W hours/kilograms, this terminal would require an unacceptable 6 kilograms of batteries for 10 hours of operation between recharges. Even with new battery technologies such as rechargeable lithium ion or lithium polymer cells, it is anticipated that the expected battery lifetime will increase to about 90-110 watt-hours/kilogram over the next 5 years which still leads to an unacceptable 3.6-4.4 kilograms of battery cells. In the future, it can be extrapolated that a large microprocessor, clocked at 500 MHz (which is a not too aggressive estimate for the next decade) would consume about 300 W. Every 10^0C increase in operating temperature roughly doubles a component's failure rate.

Low-Power Vlsi Design
Power dissipation in CMOS circuits is caused by three sources:

1) The leakage current which is primarily determined by the fabrication technology, consists of reverse bias current in the parasitic diodes formed between source and drain.
2) The short-circuit (rush-through) current which is due to the DC path between the supply rails during output transitions and
3) The charging and discharging of capacitive loads during logic changes.
4) The dynamic power dissipation and is given by:

$$P = 0.5CV_{dd}^{2}E(sw)f_{clk}$$

Where C is the physical capacitance of the circuit, V_{dd} is the supply voltage, E(sw) referred as the switching activity is the average number of transitions in the circuit per $1/f_{clk}$ time, and f_{clk} is the clock frequency.

Low power design space

Optimizing for power entails an attempt to reduce one or more of these factors.

Voltage

Because of these factors, designers are often willing to sacrifice increased The limit of how low the Vt can go is set by the requirement to set adequate noise margins and control the increase in sub threshold leakage currents. The optimum Vt must be determined based on the current drives at low supply voltage operation and control of the leakage currents. Since the inverse threshold slope (S) of a MOSFET is invariant with scaling, for every 80-100 mV (based on the operating temperature) reduction in Vt, the standby current will be increased by one order of magnitude. This tends to limit Vt to about 0.3 V for room temperature operation of CMOS circuits. Basically, delay increases by 3x for a delta V_{dd} of plus/minus 0.15 V at V_{dd} of 1 V.

Physical capacitance

Dynamic power consumption depends linearly on the physical capacitance being switched. Approximate estimates can be obtained by using information derived from a companion placement solution or by using stochastic procedural interconnect models. As with voltage, however, we are not free to optimize capacitance independently.

Switching Activity

There are two components to switching activity: f_{clk} which determines the average periodicity of data arrivals and E(sw) which determines how many transitions each arrival will generate. For circuits that do not experience glitching, E(sw) can be interpreted as the probability that a power consuming transition will occur during a single data period. Even for these circuits, calculation of E(sw) is difficult as it depends not only on the switching activities of the circuit inputs and the logic function computed by the circuit, but also on the spatial and temporal correlations among the circuit inputs.

Calculation Of Switching Activity

Delay model

Based on the delay model used, the power estimation techniques could account for steady-state transitions (which consume power, but are necessary to perform a computational task) and/or hazards and glitches (which dissipate power without doing any useful computation). Sometimes, the first component of power consumption is referred as the functional activity while the latter is referred as the spurious activity. It is shown that the mean value of the ratio of hazardous component to the total power dissipation varies significantly with the considered circuits (from 9% to 38% in random logic circuits) and that the spurious power dissipation cannot be neglected in CMOS circuits.

Power Estimation Techniques

In the following section, various techniques for power estimation at the circuit, logic and behavioral levels will be reviewed. These techniques are divided into two general categories: simulation based and no simulation based.

Simulative Approaches

A. Brute force simulation

Power Mill is a transistor-level power simulator and analyzer which applies an event-driven timing simulation algorithm (based on simplified table-driven device models, circuit partitioning and single-step nonlinear iteration) to increase the speed by two to three orders of magnitude over SPICE. Switch-level simulation techniques are in general much faster than circuit- level simulation techniques, but are not as accurate or versatile. Standard switch-level simulators (such as IRSIM) can be easily modified to report the switched capacitance (and thus dynamic power dissipation) during a simulation run.

B. *Hierarchical simulation*

A simulation method based on a hierarchy of simulators are presented in past. The idea is to use a hierarchy of power simulators (for example, at architectural, gate-level and circuit-level) to achieve a reasonable accuracy and efficiency tradeoff. Another good example is Entice-Aspen. This power analysis system consists of two components: Aspen which computes the circuit activity information and Entice which computes the power characterization data.

C. *Monte Carlo simulation*

A Monte Carlo simulation approach for power estimation which alleviates the input pattern dependence problem were also suggested. This approach consists of applying randomly generated input patterns at the circuit inputs and monitoring the power dissipation per time interval T using a simulator. Based on the assumption that the power consumed by the circuit over any period T has a normal distribution, and for a desired percentage error in the power estimate and a given confidence level, the number of required power samples is estimated.

Non-Simulative Approaches

A. Behavioral level

The power model for a functional unit may be parameterized in terms of its input bit width. For example, the power dissipation of an adder (or a multiplier) is linearly (or quadratically) dependent on its input bit width.The library thus contains interface descriptions of each module, description of its parameters, its area, delay and internal power dissipation (assuming pseudo-random white noise data inputs).

B. *Logic level*

Estimation under a Zero Delay Model Most of the power in CMOS circuits is consumed during charging and discharging of the load capacitance. Methods of estimating the activity factor E n (sw) at a circuit node n involve estimation of signal probability prob(n), which is the probability that the signal value at the node is one. Under the assumption that the values applied to each circuit input are temporally independent (that is, value of any input signal at time t is independent of its value at time t-1), we can write:

$$E_n(sw) = 2\ prob(n)\ (1 - prob(n)).$$

(2)

Computing signal probabilities has attracted much attention. In the recent years, a computational procedure based on Ordered Binary-Decision Diagrams (OBDDs) has become widespread. In this method, which is known as the OBDD-based method, the signal probability at the output of a node is calculated by first building an OBDD corresponding to the global function of the node and then performing a post order traversal of the OBDD using equation:

$$prob(y) = prob(x)\,prob(f_x) + prob(\bar{x})\,prob(f_{\bar{x}})$$

(3)

This leads to a very efficient computational procedure for signal probability estimation. The activity factor of line x can be expressed in terms of these transition probabilities as follows:

$$E_x(sw) = prob(x_{0\to 1}) + prob(x_{1\to 0})$$

(4)

The various transition probabilities can be computed exactly using the OBDD representation of the logic function of x in terms of the circuit inputs. A mechanism for propagating the transition probabilities through the circuit which is more efficient as there is no need to build the global function of each node in terms of the circuit inputs. This work has been extended to handle highly correlated input streams using the notions of conditional independence and isotropy of signals. . Given these waveforms, it is straight-forward to calculate the switching activity of x which includes the contribution of hazards and glitches, that is:

$$E_x(sw) = \sum_{t\in\, eventlist(x)} \left(prob\left(x^t_{0\to 1}\right) + prob\left(x^t_{1\to 0}\right)\right)$$

(5)

Given such waveforms at the circuit inputs and with some convenient partitioning of the circuit, the authors examine every sub-circuit and derive the corresponding waveforms at the internal circuit nodes.

Cmos Device And Voltage Scaling

In the future, the scaling of voltage levels will become a crucial issue. The main force behind this drive is the ability to produce complex, high performance systems on a chip. Two CMOS device and voltage scaling scenarios are described, one optimized for the highest speed and one trading off high performance for significantly lower power (the speed of the low power case in one generation is about the same as the speed of the high-performance case of the previous generation, with greatly reduce power consumption). It is shown that the low power scenario is very close to the constant electric-field (ideal) scaling theory.

Cad Methodologies And Techniques

Behavioral synthesis

The behavioral synthesis process consists of three steps: allocation, assignment and scheduling. These steps determine how many instances of each resource are needed, on what resource each operation is performed and when each operation is executed. This approach requires various support circuitry including level-converters and DC/DC converters. Consider a module M in an RTL circuit that performs two operations A and B. Hence, the power dissipation depends on the module binding. Similarly, consider a register R that is shared between two data values X and Y. The switching activity of R depends on the correlations between these two variables X and Y.

Logic synthesis

Logic synthesis fits between the register transfer level and the netlist of gate specification. It provides the automatic synthesis of netlists minimizing some objective function subject to various constraints. Depending on the input specification (combinational versus sequential, synchronous versus asynchronous), the target implementation (two-level versus multi-level, unmapped versus mapped, ASICs versus FPGAs), the objective function (area, delay, power, testability) and the delay models used (zero-delay, unit-delay, unit-fanout delay, or library delay models), different techniques are applied to transform and optimize the original RTL description.

Physical design

Physical design fits between the netlist of gates specification and the geometric (mask) representation known as the layout. It provides the automatic layout of circuits minimizing some objective function subject to given constraints. Depending on the target design style (full-custom, standard-cell, gate arrays, FPGAs), the packaging technology (printed circuit boards,

multi-chip modules, wafer-scale integration) and the objective function (area, delay, power, reliability), various optimization techniques are used to partition, place, resize and route gates.

Power Management Strategies

In many synchronous applications a lot of power is dissipated by the clock. The clock is the only signal that switches all the time and it usually has to drive a very large clock tree. Moreover in many cases the switching of the clock causes a lot of additional unnecessary gate activity. For that reason, circuits are being developed with controllable clocks.

TRANSITION POWER OPTIMIZATION USING LAGGER ALGORITHM

Bus transition logic

Activation of external buses consumes significant power as well, because many input–output (I/O) pins and large I/O drivers are attached to the buses. Typically, 50% of the total power is consumed at the I/Os for well-designed low-power chips by R.Wilson. Thus, reducing the power dissipated by buses becomes one of the most important concerns in low-power VLSI design. The dynamic power dissipated in a bus is expressed as the following;

$$P_{\mathrm{BUS}} = \sum_{\mathrm{line}} C_{\mathrm{load}} V_{\mathrm{DD}}^2 N_{\mathrm{trans}}$$

Where C_{load} is the total load capacitance attached to a bus line, V_{DD} is the voltage swing at operation, and N_{trans} is the number of transitions per second. There are two approaches to reduce the dynamic power of buses. One is to save the dynamic power per activation by reducing either C_{load} or V_{DD}.

Sequence-switch coding

The I/O data are transferred consecutively at a relatively constant rate. This kind of transfer pattern gives us a new opportunity to reduce the number of bus and I/O) transitions during data transmission. When a sequence of data moves through a bus, its transmission sequence can be chosen to minimize the number of bus transitions. For example, the effect of the sequence on the number of bus transitions is illustrated in Fig. 1. Let us assume that there are eight data to be sent via a bus, and Fig. 3.1(a) is the waveform of the bus when these are transmitted without any modification.

Resistive Feedback Power Optimization

Logical modeling

The formulation might become non-linear, since changing the W/L ratio of a MOSFET changes the channel resistance as well as the associated parasitic capacitances Thus, an n-diffusion capacitor and a resistor wire with a blocking mask is developed. The blocking mask increases the resistivity of the polysilicon resistor. To simulate a realistic situation, each delay element is driven by an inverter gate and is also loaded with an inverter. The circuit set up is shown in Figure1.The inverter and the transmission gate cells are made of transistors with minimum sizes.

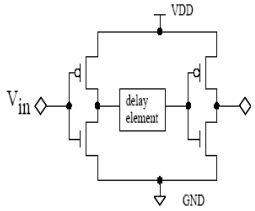

Figure 1. Circuit setup for resistive load placement

The delay/power (metric 1) and delay/area (metric 2) are used as the referencing values for power minimization. The delay values used to calculate both metrics are given in column 2 of the table 1. The power consumption values used to calculate metric 1 are expressed in μW. Since the delay elements are implemented as standard cells with fixed height, the area is measured in terms of the number of grid units along the width. This delay element is called as resistive feedthrough logic. The resistance of a rectangular slab of length L, width W and thickness t can be calculated in terms of a material specific constant called resistivity ρ, as R=ρL/(Wt).

Glitch free physical design

The resistances found from the lookup table are automatically designed as standard cells. These feedthrough cells are inserted into the original circuit by modifying a HDL netlist of the circuit. The place-and-route layout of the modified netlist is then done using a commercial tool such as Tanner.

DESIGN IMPLEMENTATION

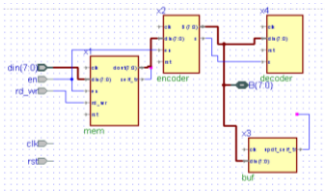

Figure 2. Implemented system diagram on Aldec's Block diagram

Result Analysis

For the evaluation of the suggested approach an simulation is carried out in Active HDL tool and then the units are developed on tanner tool for the glitch minimization. The obtained simulation results are as shown below,

With stray capacitance:

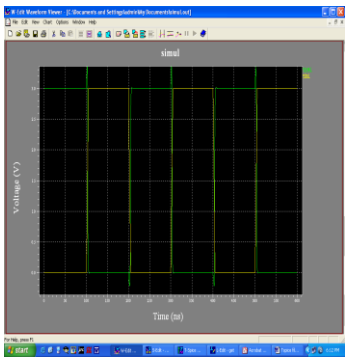

Figure 3. Simulation observation with stray capacitance

After feed-back path offered:

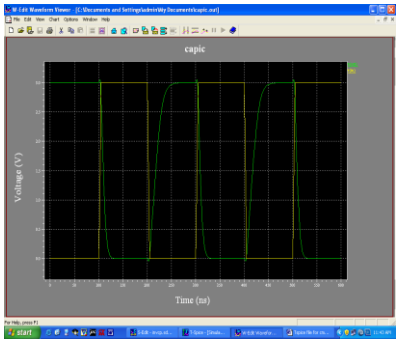

Figure 4. Spice simulation showing the glitch minimization

DEVICE UTILIZATION SUMMARY

Selected Device: 2vpx70ff1704-7

Number of Slices	: 11533 out of 33088	34%
Number of Slice Flip Flops	: 571 out of 66176	0%
Number of 4 input LUTs	: 20312 out of 66176	30%
Number of bonded IOBs	: 326 out of 996	32%

Number of GCLKs : 1 out of 16 6%

CONCLUSION

The Low power-designing objective is successfully developed based circuit level and behavioral level design flow. This was done without re-design of the CMOS logic with resister feedback. The new design flow is effective in designing minimum transient energy standard cell based digital CMOS circuits. The objective is achieved with CMOS level developing on Tanner CAD tool and simulating it on Spice simulator. The power optimization is also achieved by using Bus transition minimization where a Lagger algorithm is realized for the minimization of transitions to reduce power consumption in Bus architecture.

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