LOW POWER WITH IMPROVED NOISE MARGIN FOR DOMINO CMOS NAND GATE

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ABSTRACT
With the advancement in semiconductor technology, chip density and operating frequency are increasing, so the power consumption in VLSI circuits has become a major problem of consideration. More power consumption increases packaging cost and also reduces the battery life of the devices. So it has become necessity of the VLSI circuits to reduce the dynamic as well as the static power consumption. To reduce leakage power it is necessary to increase the threshold voltage of the circuit. In this paper to reduce the leakage power AVL (Adaptive Voltage Level) circuit technique and Body biasing technique are used. Our paper proposes a technique for reducing power dissipation of CMOS VLSI design while simultaneously improving the noise immunity.

Keywords: AVL circuit technique, CMOS, Noise immunity, VLSI circuit.

INTRODUCTION
It is important to introduce low-power design techniques and to reduce the package size during the circuit normal mode of operation. More power consumption also reduces the battery life of the devices. Therefore reducing power dissipation during operation has become a critical objective in today's VLSI circuit designs. So special cooling equipment is necessary to remove excessive heat produced during circuit operation. Power consumption in CMOS circuits can be dynamic or static. Dynamic power dissipation takes place due to switching activities because of short circuits current and charging and discharging of load capacitances. Static power consumption is another type of power dissipation in CMOS circuits. Leakage currents with sub-threshold source-to-drain leakage, reverse bias junction band-to-band tunneling, gate oxide tunneling, and other current drawn continuously from the power supply cause static power dissipation [7].

Today, the necessity of portable systems and simultaneously improvement in battery performance depicts the power consumption is major factor in CMOS VLSI design parameters [3]. To reduce dynamic power dissipation it is necessary to reduce the supply voltage of the circuit, reduction of supply voltage after a certain limit affects the performance of the circuit, to maintain circuit performance of the circuit it is necessary to decrease the threshold voltage as well, but it leads to leakage power dissipation. Leakage power can be reduced by increasing the threshold voltage [5]. In this paper to reduce the voltage applying to the load circuit, we suggest the use of AVL (Adaptive Voltage Level) circuit technique. AVL circuit is controlled by sleep control signal. The advantage of using AVL circuit is that the load circuits can operate quickly when they are in active mode due to the increase in drain-source current as the AVL circuit supplies the maximum drain-source voltage Vds to the on-MOSFETS through on-switches. On the other hand, during standby mode, it supplies a slightly lower voltage through the weakly-on switches [2]. Hence the sub-threshold leakage current of the off-MOS transistors decrease and the standby power gets reduced. It also produces high noise immunity. When we applied voltage to the substrate of a MOSFET it affects the threshold voltage of a MOSFET as well. The voltage difference between the source and the substrate, V_{BS} also affects the width of the depletion layer and due to changes in the charge in depletion layer voltage across the oxide also get changed. Therefore the expression for the threshold voltage is given by:

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_s q N_a (2\phi_F + V_{SB})}}{C_{ox}}$$

The threshold difference due to an applied source-substrate voltage can therefore be expressed by:

$$\Delta V_T = \gamma(\sqrt{(2\phi_F + V_{SB})} - \sqrt{2\phi_F})$$

Where γ is the body effect parameter given by:

$$\gamma = \frac{\sqrt{2\varepsilon_s q N_a}}{C_{ox}}$$

Substrate biasing provides an effective circuit-level technique for varying threshold voltage and to enhance the performance of the circuit.

This paper gives emphasis on low power design as well as improved noise margin for domino NAND gate technique. Among different dynamic logic circuit techniques, domino logic technique is mostly used because it provides less delay and its area consideration, but it has less tolerance to noise and its static power consumption is high. So in this paper we have applied AVL circuit technique and body bias technique to overcome both of these problems.

STANDARD DOMINO NAND GATE

A standard domino NAND gate is as shown in Figure 1. A standard Domino NAND gate consists of one p-type transistor and an n-type dynamic logic block. During pre-charge phase the output node of the dynamic CMOS stage is pre-charged to high logic level [4]. During evaluation phase, the output node of the dynamic CMOS stage is either discharged to a low level or it remains high, means that, the output node may be selectively discharged through the n-type logic block depending upon whether there is a path exist to the GND or not. It depends upon the inputs of the NMOS logic block. If a path to ground is not formed during the evaluation phase, means there is no conducting path exist to the ground, we get the high logic level at the output. If inputs to the n-type logic blocks are such that it makes a conducting path to the ground, output will be low.

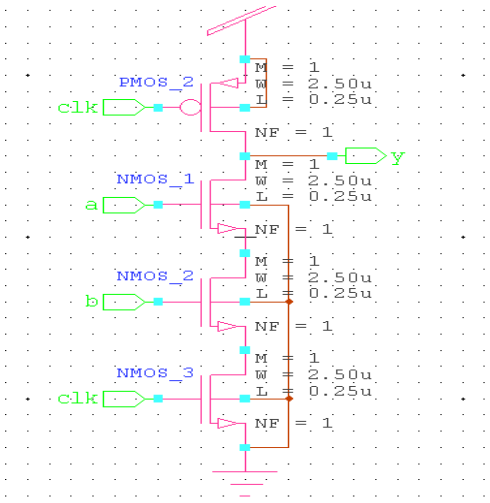

Figure 1 Domino NAND GATE

AVL NAND GATE

In this circuit AVL circuit is connected above the Domino NAND gate. AVL circuit contained one p-MOSFET and two series connected n-MOSFETS, which will reduce the voltage applying to the load circuit. AVL circuit is controlled by sleep (slp) control signal [1]. When sleep signal is low, the p-MOSFET is on, while series connected n-MOSFETs are off. During this operation, we get the full voltage out of the AVL circuit. When sleep signal make transition from low to high, this will turn-on series connected n-MOSFETs, and turn-off p-MOSFET, Thus, the drain-to-source voltage (Vdsn), of the off n-MOS in load circuit (domino NAND gate) can be expressed as

$$Vdsn = VDD - 2v$$

Where v is a voltage drop of the series connected single n-MOSFET and Vdsn can be changed by changing the number of series connected n-MOSFETs. If Vdsn decreases this will increase the barrier height of the off n-MOS [6], therefore it will decrease the drain induced- barrier-lowering (DIBL) effect and, consequently, increase Vthn. This result in a decrease in the sub threshold current of the n-MOS, therefore the leakage current through the gate decreases.

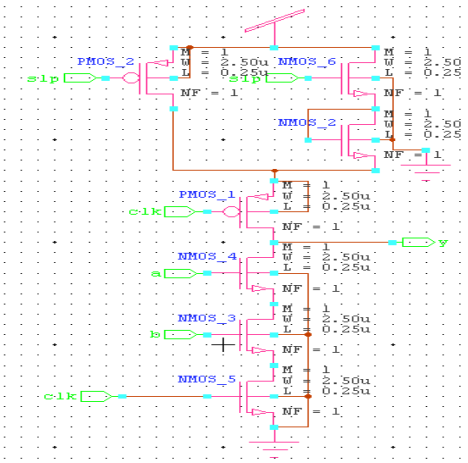

Figure 2 AVL NAND GATE

BODY BIAS NAND GATE

Domino logic gates are frequently employed in high performance circuits for high speed and area efficiency. As supply voltage is reduced, delay increases, unless threshold voltage Vth is also decreased. Substrate biasing provides an effective circuit-level technique for varying threshold voltage. Here substrate of NMOS is connected to the clock and PMOS is connected to Vdd, which increases the threshold voltage that in turn reduces the leakage current.

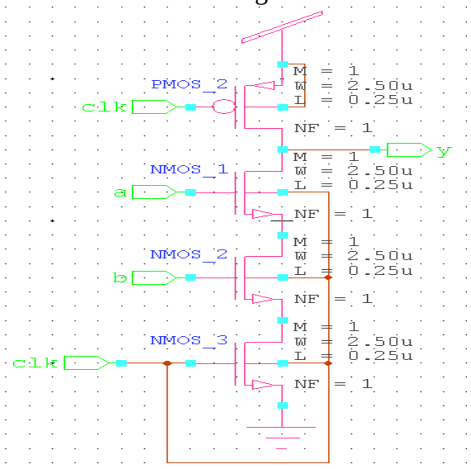

Figure 3.Body Bias NAND GATE

NAND GATE USING PROPOSED TECHNIQUE

In this method we have taken Domino NAND gate with both of the techniques, AVL circuit technique and body biasing technique. Here AVL circuit is connected above the NAND gate. For applying body bias technique, the substrate of PMOS is connected to Vdd and the substrate of NMOS is connected to the clock. Our proposed method will reduce the power consumption through the gate. Simulations of all the circuits are performed using Tanner EDA Tools 180 nm technology. The advantage of using AVL circuit is that load circuit will operate very fast when they are in active mode due to increase in drain source current but in stand by mode due to less drain source voltage, threshold voltage will increase which reduces the leakage current, of the circuit [1].

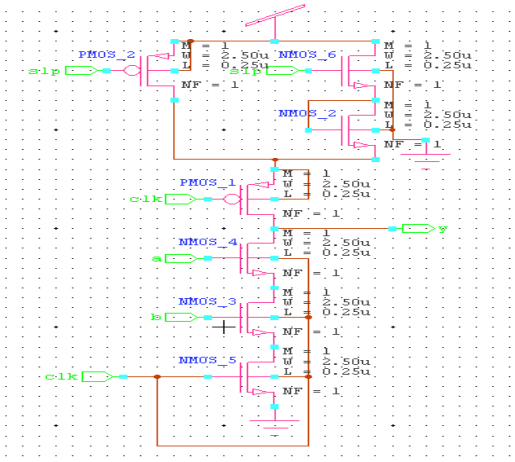

Figure 4.Proposed NAND GATE

Parameters Observation

The parameters observations of different techniques are as follow:

Technique	Dynamic power dissipation In mili watts	Leakage Power in pico watts	Evaluation Delay in Pico seconds	Noise margin in volts (NMH)	Noise margin in volts (NML)
Domino NAND gate	0.087	140.73	25.99	1	0.5
AVL NAND gate	0.068	162.20	37.58	1	0.5
Body Bias NAND gate	0.081	176.95	25.81	1.2	0.85
Proposed NAND gate	0.052	130.70	36.42	1.6	0.85

Table 1.Parameters observation

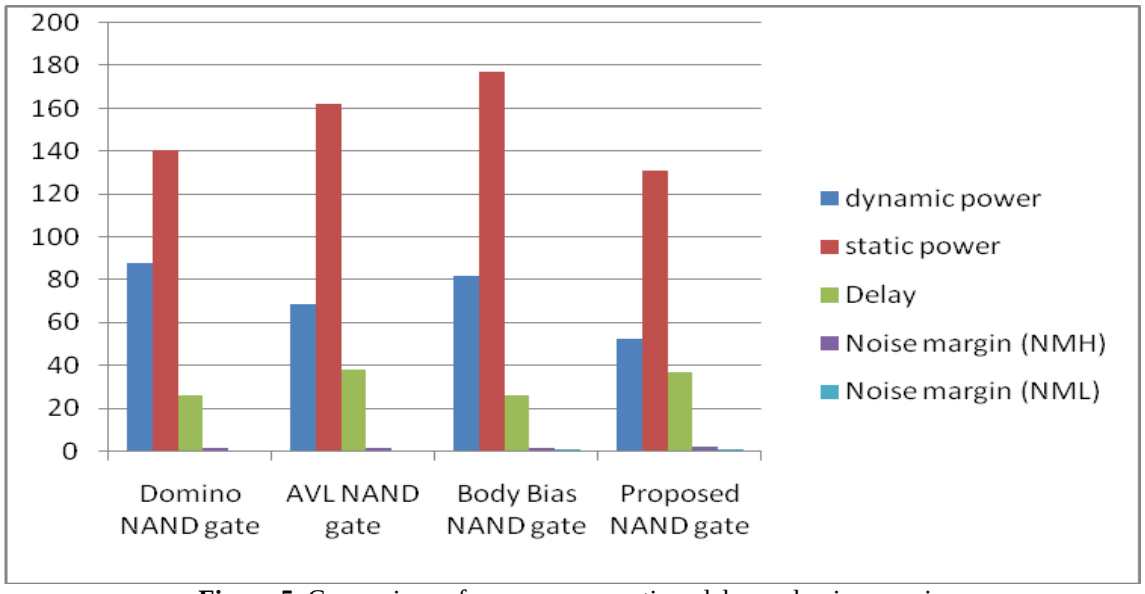

Figure 5. Comparison of power consumption, delay and noise margin

SIMULATION RESULTS

The output of the domino NAND GATE is shown below

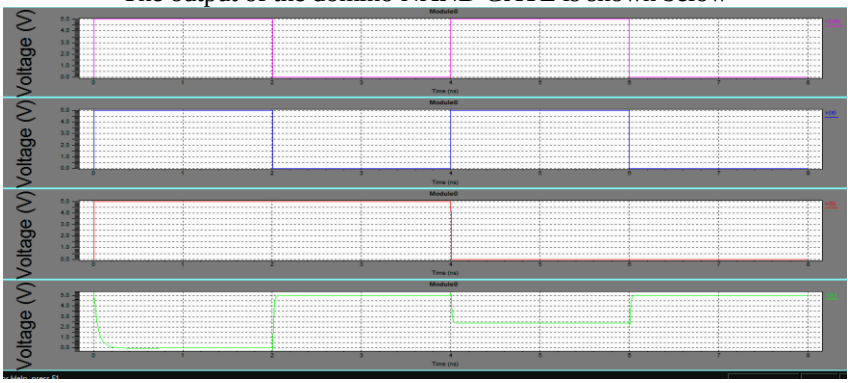

Figure 6 Domino NAND GATE

The output of the AVL NAND GATE is shown below

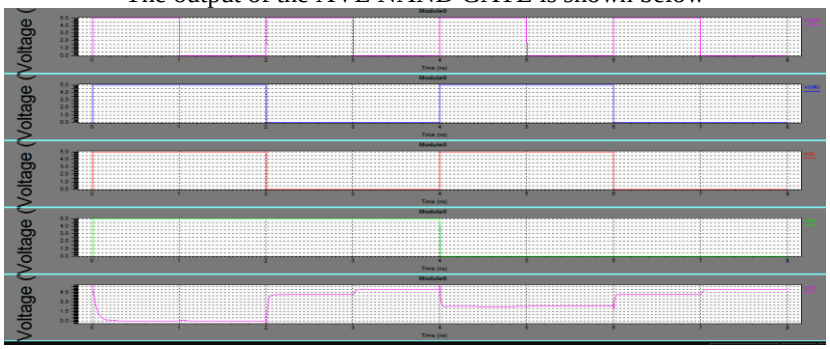

Figure 6.AVL NAND GATE

The output of the body bias NAND GATE is shown below

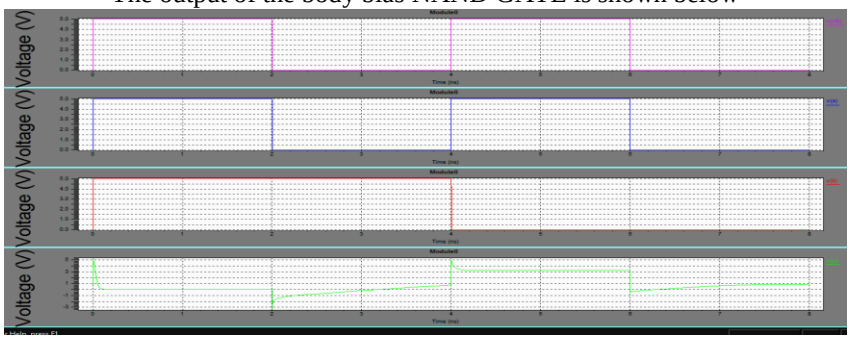

Figure 7.Body bias NAND GATE

The output of the proposed NAND GATE is shown below

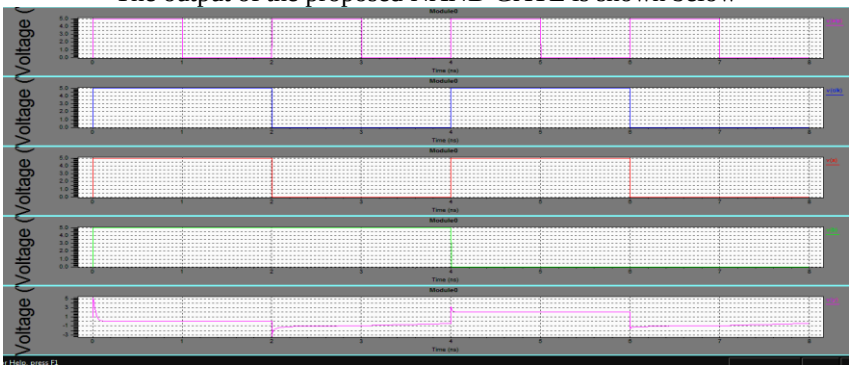

Figure 8.Proposed NAND GATE

CONCLUSION

In this paper we have designed Domino NAND gate with AVL circuit technique and body bias technique, and comparison has been carried out with standard domino NAND gate, AVL NAND gate and body bias NAND gate.
Simulation results shows that our proposed circuit technique consumes less dynamic as well as static power than other three techniques. The other benefit of proposed technique is its high noise immunity as compare to other technique.

In this dissertation we can say that our proposed NAND gate consumes less power and gives high noise margin.

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