2^n:1 Reversible Multiplexer and its Transistor Implementation

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Abstract:
The advantages of reversible logic systems and circuits have drawn a significant interest in recent years as a promising computing paradigm having applications in low power CMOS, quantum computing, nano technology, digital signal processing, computer graphics, cryptography and optical computing. In this paper, new reversible PV gate is proposed and the design of 2:1, 4:1 and 8:1 reversible multiplexer using the proposed reversible gate is discussed. Transistor implementation of proposed gate is done using virtuoso tool of cadence. Based on the result of the analysis, some of the trade-offs are made in the design to improve the efficiency.

Keywords- Basic reversible gates; Constant inputs; Reversible Multiplexer; Garbage; Gate count; Transistor count.

I. INTRODUCTION

The key components of communication systems are a multiplexer (Mux, parallel-to-serial converter) and a Demultiplexer (De-Mux, serial-to-parallel converter). In conventional computers, the computation carrying out is irreversible i.e. once logic block generates the output bits, the input bits are lost. But it is not in the case of reversible logic circuits. The classical set of gates such as AND, OR, and EXOR are not reversible as they are all multiple-input single output logic gates.

A gate is reversible if the gate's inputs and outputs have a one-to-one correspondence, i.e. there is a distinct output assignment for each distinct input. Therefore, a reversible gate's inputs can be uniquely determined from its outputs. Reversible logic gates must have an equal number of inputs and outputs [9]. Then the output rows of the truth table of a reversible gate can be obtained by permutation of the input rows. Reversible logic circuits have emerged as a promising technology in the field of information processing.

Irreversible hardware computation results in energy dissipation due to information loss [2]. According to the Landauer [6], traditional irreversible hardware computation inevitably leads to energy dissipation due to the loss of each one bit of information which dissipates an amount of KT ln(2) joules of energy, where K is the Boltzmann's constant and T is the absolute temperature at which computation is performed. This erasure is not done significantly and more power is dissipated for each erased bit. Power dissipation which leads to overheating is one of the major concerns in modern technologies. Thus, an alternative logic operation known as reversible logic came into existence, which does not erase information and also dissipate arbitrarily less heat [10].

Charles Bennett proposed a theoretical background which proved that reversible general purpose computing devices can be built [2, 3]. This gave rise to reversible logic circuits. Logical reversibility means that after finishing a computation, it is possible to retrace every step and reconstruct data which was used in every step. Thus, reversible logic circuits offer an alternative that allows computation with very small energy dissipation [17].

There is number of existing reversible gates in literature like Fredkin, Feynman and Toffoli gates etc. Experimental reversible chips and arithmetic circuits have been developed recently as well as magnetic, Josephson junction, nano-electronic and quantum implementations of reversible logic circuits have been proposed in different literatures [4-15]. Photon being the ultimate unit of information with unmatched speed and with data package in a signal of zero mass, the techniques of computing with light may provide a way out of the limitations of computational speed and complexity inherent in electronics computing. Different optical logic gates have already been proposed to perform irreversible logic function. But, reversible computation in a system can be performed if the system is composed of reversible gates. The well known 2x2 Feynman [14] gate operates as a controlled NOT (CNOT) if the control input of CNOT is set '0', the gate acts as a BUFFER gate; else, it acts as a NOT gate. The Feynman gate can be used as fan-out gate to copy a signal. Toffoli [20] and Fredkin gates are 3x3 reversible gates. Each of these gates is universal, i.e. any logical reversible circuit can be implemented using these gates.

II. BASIC REVERSIBLE LOGIC GATE

A set of reversible logic gates is needed to design reversible logic circuits. An N*N reversible logic gate can be represented as:

$$I_V = (I_1, I_2 \ldots\ldots, I_N)$$
$$O_V = (O_1, O_2 \ldots\ldots, O_N) \quad (1)$$

Where, I_v and O_v are inputs and output vectors. Consider following issues to perform synthesis of reversible gates and obtain optimization

- Garbage: Garbage is the number of outputs added to make an n-input k-output Boolean function ((n,k) function) reversible. In other sense, a reversible logic gate has an equal number of inputs and outputs (k*k) and all the outputs are not expected. Some of the outputs should be considered to make the gate reversible and those undesired outputs are known as garbage outputs. A heavy price is paid for every garbage outputs.
- Gate count: The number of reversible gates used to realize the function [11].
- Flexibility: This refers to the universality of a reversible logic gate in realizing more functions [12].
- Transistor Count: It denotes the effort needed, to realize a reversible circuit. The transistor count of a reversible gate is the number of transistors used in the gate [16].
- Critical path: Delay can be calculated in reversible logic based on the critical path. It is the longest path in the system to get the desired output [13].

Several reversible logic gates have been proposed. Among them a general New Toffoli Gate, NTG [8], New Gate, NG [5, 7], TKS Gate [18], TR gate [19] are discussed.

III. DESIGN OF REVERSIBLE MULTIPLEXER

We design the reversible circuit using dual-line pass-transistor logic [1] and monotone circuit. Boolean values X=1 and X=0 are denoted by (X,X)=(1,0) and (X,X)=(0,1), respectively. For example, an inverter is shown in Fig 1. It consists of a metal cross-over. Because of the monotone circuit, we set all initial values (X,X) = (0,0).

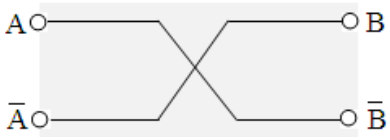

Figure.1. Reversible inverter

For the implementation of an on-off switch, we use a CMOS transmission gate which is a two-way switch shown in Figure. 2.

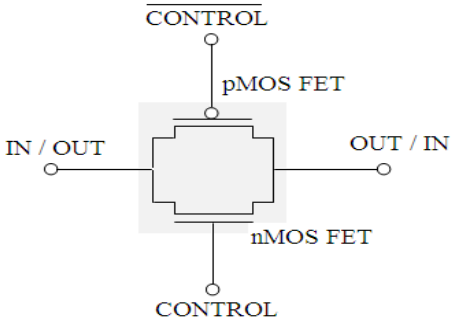

Figure..2. CMOS Transmission gate

IV. PROPOSED REVERSIBLE MULTIPLEXERS

A. 2:1 Reversible Multiplexer

A 3x3 reversible PV gate is proposed in order to function as the 2:1 reversible multiplexer producing two garbage bits. The inputs are S, A and B. Based on the selection input S, the corresponding message bits are passed on to the output 'Y'. Figure 3 depicts the symbolic representation of PV gate and Table I describes its truth table.

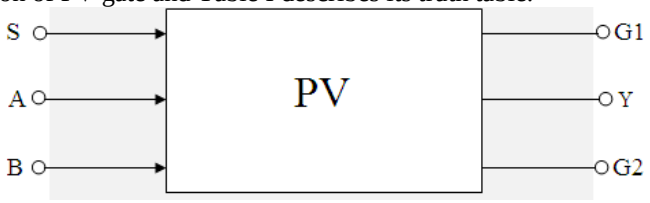

Figure.3. Reversible PV gate functioning as 2:1 reversible multiplexer

TABLE I. TRUTH TABLE OF REVERSIBLE PV GATE

S	*A*	*B*	*G1*	*Y*	*G2*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

When the select input S=0, the output Y follows the input A, i.e Y=A, if the S=1, then the output Y follows the input B, i.e Y=B. 'G1' and 'G2' are the two garbage bits which is not required in multiplexing operation. However G1 follows the select input S, it may be used in additional circuits which requires the same input.

B. Design of 4:1 Reversible Multiplexer using reversible PV gate

Using the proposed reversible PV gate, 4:1 multiplexer can be designed as shown in Figure 4. This design requires three PV gates such that producing six garbage outputs. The Table II describes the truth table of 4:1 reversible multiplexer, the garbage outputs are discarded as it doesn't play a vital role in the multiplexing operation.

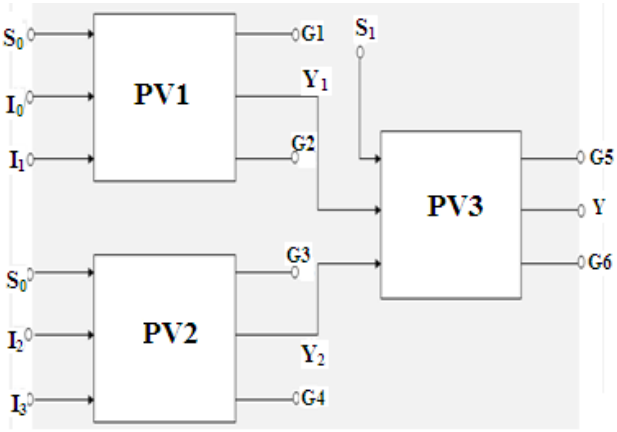

Figure.4. Design of 4:1 reversible multiplexer using PV gate

TABLE II. TRUTH TABLE OF REVERSIBLE 4:1 MULTIPLEXER

Select Inputs		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

The above truth table depicts there is no change in the functionality of 4:1 reversible multiplexer with respect to the irreversible multiplexer functionality. The equation for the output 'Y' is given as follows,

$$Y = \bar{S}_1\bar{S}_0I_0 + \bar{S}_1S_0I_1 + S_1\bar{S}_0I_2 + S_1S_0I_3$$

C. Design of 8:1 Reversible Multiplexer using reversible PV gate

Using the same proposed PV gate 8:1 reversible multiplexer also can be designed as shown in Figure 5 and Table III shows its truth table. This design uses seven PV gates producing 14 garbage outputs. In general we can design 2^n:1 reversible multiplexer where n is 1, 2, 3…n. For 2^n:1 reversible multiplexer (2^n-1) PV gates are required producing 2*(2^n-1) number of garbage outputs.

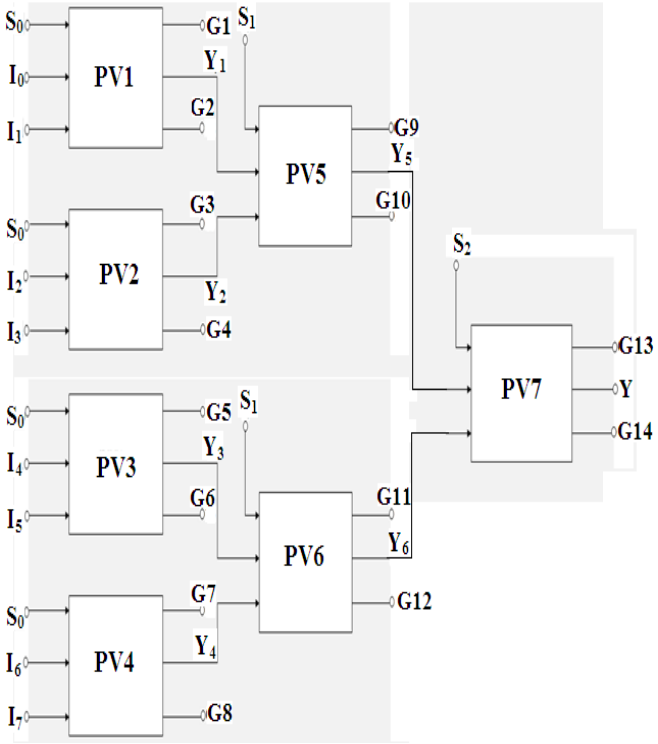

Figure.5. Design of 8:1 reversible multiplexer using PV gate

TABLE III. TRUTH TABLE OF REVERSIBLE 8:1 MULTIPLEXER

Select Inputs			Output
S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

$$Y = \bar{S}_2\bar{S}_1\bar{S}_0I_0 + \bar{S}_2\bar{S}_1S_0I_1 + \bar{S}_2S\bar{S}_0I_2 + \bar{S}_2S_1S_0I_3$$
$$+S_2\bar{S}_1\bar{S}_0I_4 + S_2\bar{S}_1S_0I_5 + S_2S_1\bar{S}_0I_6 + S_2S_1S_0I_7$$

V. IMPLEMENTATION OF PV GATE

The proposed reversible PV gate is realized using transistor implementation as described in Figure 6, Figure 7 and Figure 8. To construct one reversible PV gate five transistors are required. The required output 'Y' can be obtained using only two transistors however the other three transistors are required for calculating garbage outputs. To obtain output G1, a pass transistor is used for passing the selection input S to the output G1 as shown in Fig 8.

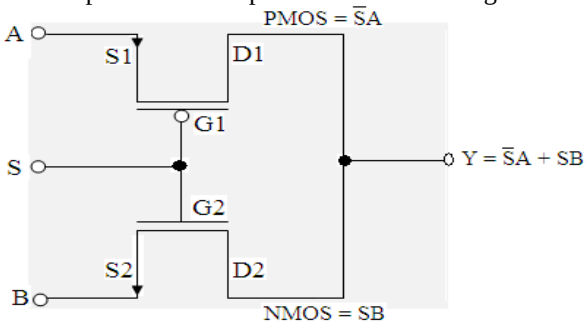

Figure.6. Circuit diagram for multiplexed output Y

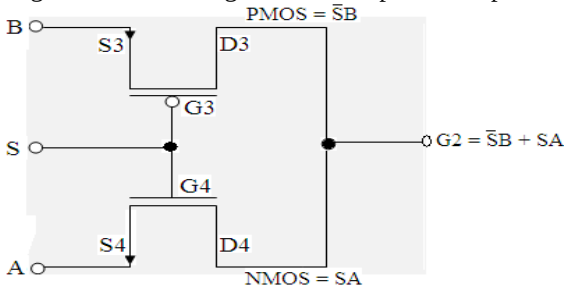

Figure.7. Circuit diagram for output G2

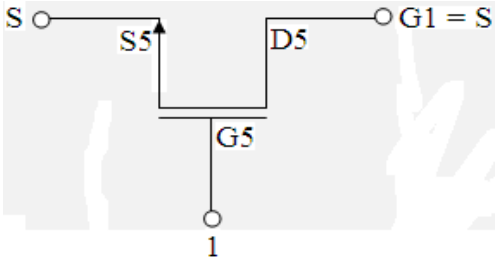

Figure.8. Circuit diagram for output G1

In Fig 6, when the selection input is 0, the pmos transistor will be ON while nmos will be off thus input A is passed to the output Y. If the selection input is 1, then nmos transistor will be conducting while pmos is in OFF state, passing input B to the output Y. Similar to output Y, output G2 is passed with input B when S=0 and input A when S=1.

VI. IMPLEMENTATION OF PV GATE

The proposed reversible PV gate is realized using the virtuoso tool of cadence. Spectre simulator of cadence is used to simulate the output. The simulations are performed using the 0.18uM technology. The circuit implementation of PV gate is shown in Figure 9. The input and output waveforms simulated for the PV gate is shown in Figure 10.

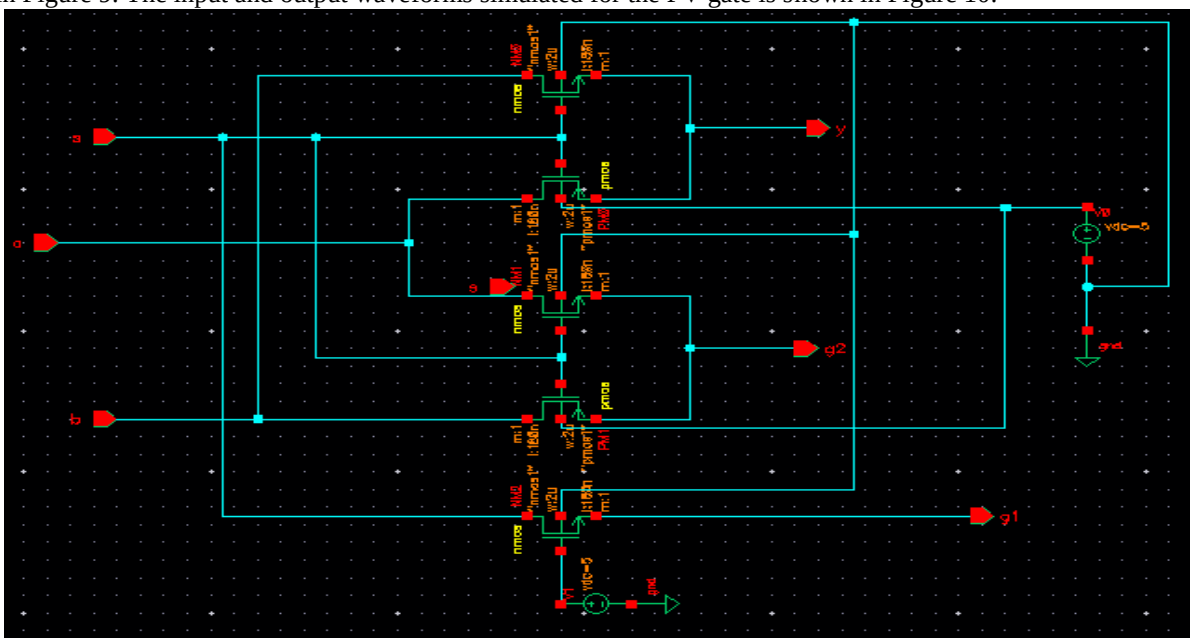

Figure.9. Transistor implementation of PV gate as 2:1 reversible multiplexer

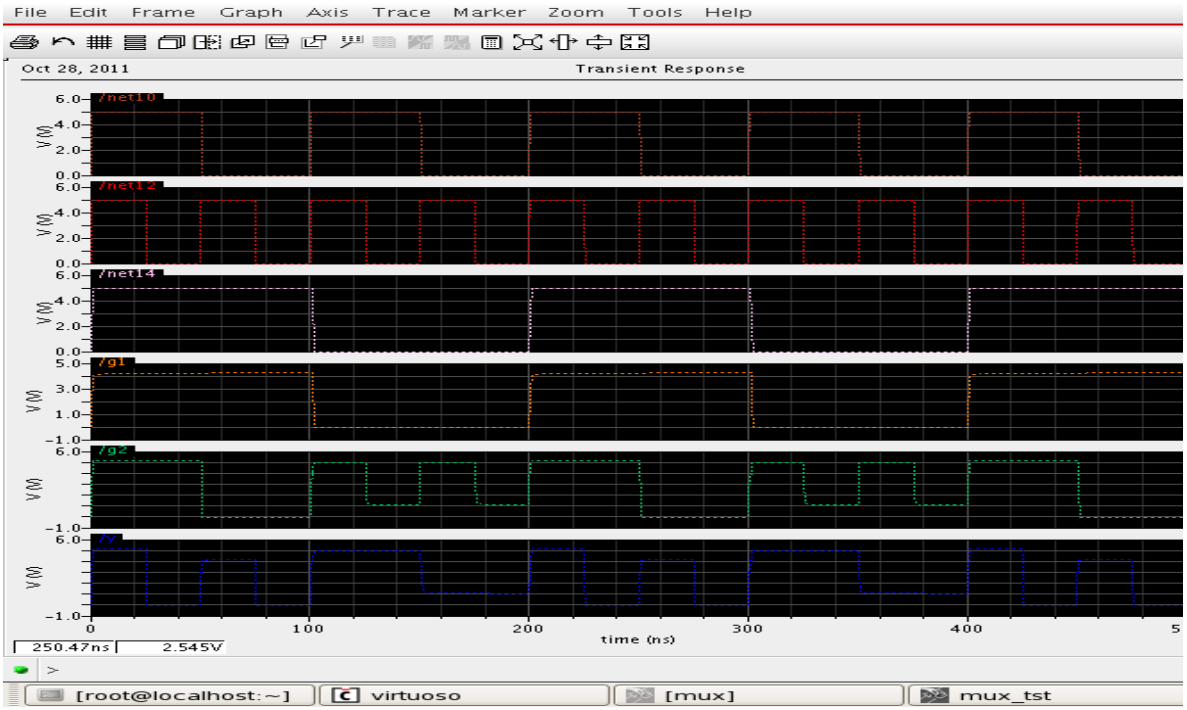

Figure.10. Simulation output of PV gate

VII. CONCLUSION

In this paper, the reversible multiplexer using PV gate is proposed and described. Simulation result and transistor implementation confirming described method is also presented in this paper. It is worth noting that the synthesis of reversible logic is different from irreversible logic synthesis. One of the major constraints in reversible logic is to minimize the number of reversible gates used, garbage outputs produced and usage of number of constant inputs. The proposed 2^n:1 reversible multiplexer requires (2^n-1) PV gates producing 2*(2^n-1) number of garbage outputs, where n is 1, 2, 3 … n.

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